Applying photolithography-friendly design to e-beam direct writing for 65-nm node and beyond

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ABSTRACT

It is commonly known that maskless lithography is the most effective technology to reduce costs and shorten the time need for recent photo-mask making techniques. In mass production, however, lithography using photo-masks is used because that method has high productivity. Therefore a solution is to use maskless lithography to make prototypes and use optical lithography for volume production. On the other hand, using an exposure technology that is different from that used for mass production causes different physical phenomena to occur in the lithography process, and different images are formed. These differences have an effect on the characteristics of the semiconductor device being made. An issue arises because the chip characteristics are different for the sample chip and the final chip of the same product. This issue also requires other processes to be changed besides switching to the lithography process. In our previous paper, we reported on new developments in an electron-beam exposure data-generating system for making printed images of a different exposure source correspond to each other in lithographic printing systems, which are electron beam lithography and photolithography. In this paper, we discuss whether the feasibility of this methodology has been demonstrated for use in a production environment. Patterns which are generated with our method are complicated. To apply the method to a production environment we needed a breakthrough, and we overcame some difficult issues.

Keywords: Maskless lithography, E-beam exposure, Photolithography, Lithography simulation, Low volume production

1. INTRODUCTION

Faster development of products is increasingly in demanded because of the growing diversification of the electronics market. Quickly producing small lots of prototype chips is increasingly required for system LSIs that are made using leading-edge semiconductor process technologies, in order to test their functions and performance in actual products. In view of these trends, maskless lithography can create a development environment that can reduce costs and shorten production periods. In mass production, however, lithography that uses photo-masks is employed because that method has high productivity. Using a different exposure technology causes different physical phenomena in the lithography process, which results in different images being formed on the wafers. We showed the resist patterns that form in electron beam (e-beam) exposure and optical exposure, and we revealed the effect caused by differences in the manufacturing processes of e-beam exposure and optical exposure in a previous paper [1]. Moreover, we proposed a data-processing method for making the printed image correspond even though they were produced in different lithographic printing systems, namely e-beam lithography (EBL) and photolithography using a different exposure source. We finished our basic examination of the data-processing method, and our true aim was to develop semiconductor devices that cost less than those made using only optical lithography, by using EBL together with optical lithography.

In this paper, we discuss whether the feasibility of this methodology has been demonstrated for use in a production environment. Theoretically, there is hardly any limit to generating e-beam exposure data for target images. In reality, however, there are many problems when doing this in a production environment. First we show the concept of generation e-beam exposure data in practical applications, and then show how this leads to the best way to get e-beam exposure data. Next, we define criteria for judging the feasibility of this method. Then, we examine the printability on a wafer. Finally, we investigate the feasibility of applying our methodology to mass production.

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2. BACKGROUND

There are many development stages to go through before a semiconductor device is shipped. These processes are shown in Fig. 1. The development of devices cannot be completed only with experiments in computation. Experiments in production processes are also needed for things such as making a feasibility study or reducing the debugging time. For example, experiments are done during R&D for litho-model designs, in elemental designs for evaluating whether products meet the specifications, or in making prototype chips for function or performance testing. Before producing the end products, many expensive mask sets are fabricated for low-volume production and are consumed in the short term. Total cost to produce low-volume parts such as most ASIC designs is dominated by mask costs [2]. For example in 65-nm process generation, a mask set is priced at $2 million and takes two weeks to prepare. Maskless lithography is the most effective technology for this low-volume production. We recommend using EBL for low-volume production and photolithography for high-volume production.

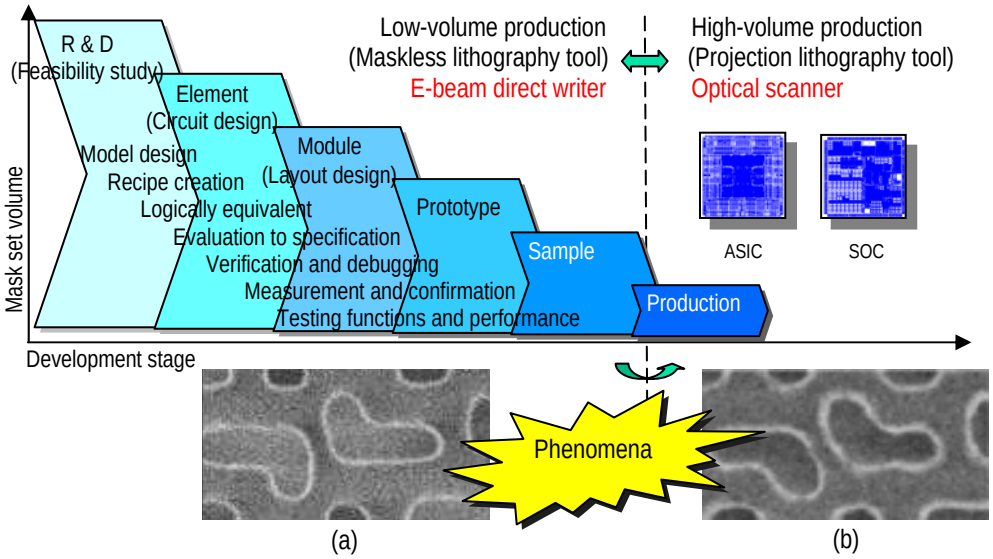

Fig. 1. Relation between device development stages and lithography tools, and comparison of the shape of resist patterns between electron beam and ArF exposure: (a) SEM image by electron beam exposure; (b) SEM image by ArF.

2.1 Printability problems

The Scanning Electron Microscope (SEM) images in Figs. 1(a) and 1(b) show the resist patterns produced in both EBL and photolithography when the same design data was exposed. As can be seen from these SEM images, EBL has better printability than photolithography. The accuracy of the transistor shape or wire width is a factor that has a significant effect on the device characteristics as illustrated in Figs. 2(a) and 2(b). However, we regard these different images as a serious problem. We have realized that the chip actually works less well when EBL is used to make a better pattern in terms of the quality of the lithography. This is because at 65-nm node and beyond, the chip characteristics are based on not only the pattern of the design data, but also on the pattern made by the photolithography. It becomes more and more difficult for photolithography to make a pattern that matches the design, and device parameter extraction has to consider this aspect of photolithography. With 65-nm node, the line is less than one-third of the effective wavelength. As the industry moves forward, optical diffraction and interference are becoming fundamental obstacles [3]. Therefore, design for manufacturability (DfM) or manufacture-aware design (MAD) is becoming indispensable [4, 5, 6], and tape-out data is designed to prevent this unique effect of photolithography regardless of the unique effect of EBL. Moreover, on a fabrication line, conditions of several processes that a product undergoes after lithography are tuned so that they give a

similar result as photolithography. Therefore, at the end of the fabrication line, a better pattern produced by EBL is not maintained. Another big issue is that the chip characteristics of a sample chip and a final chip are different for the same product.

2.2 Purpose and solution

Our previous work finished making a basic examination of our technique in which we can obtain the same shapes even if we use different lithographic technologies by improving the design data based on photolithography. We call it "PLFD (Photolithography-friendly design)." The modified patterns produced with PLFD are almost the same as the original design patterns in photolithography. By using this PLFD technique, no additional changes are required except for switching to the lithography process.

EBL draws patterns more precisely than photolithography; in the case of a square pattern, for example, e-beam draws it almost as a square form, while photolithography draws it as a circle. It is evident from the illustrations in Fig. 2(c) that the number of vertexes increases dramatically, because the pattern data of a PLFD design is inputted into EBL so that EBL reproduces the image of photolithography. The PLFD patterns consist of complicated shapes and have a large number of minute edges and vertexes. The purpose of our present work is to find a method to apply PLFD to a production environment and to confirm that it is feasible.

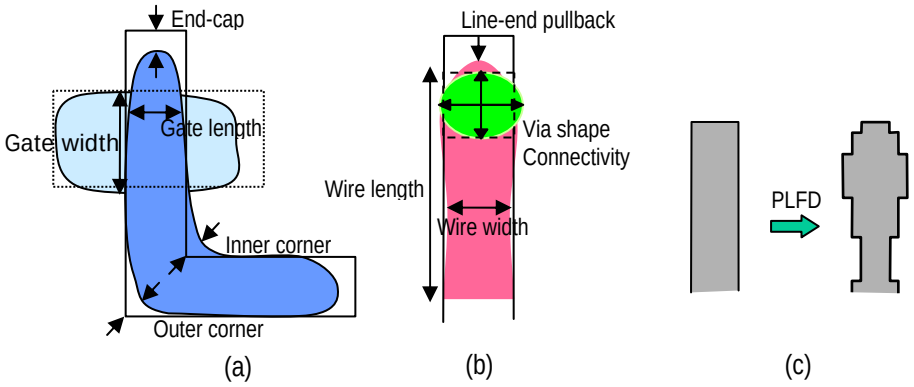

Fig. 2. Printability problems and Photolithography-friendly design. (a) Transistor shape has effects on transistor characteristics; Vth, Ion, and Ioff. (b) Wire shape has effects on wire characteristics; Capacitance, Resistance, Via resistance, and Dielectric. (c) Schematic illustration of PLFD

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3. METHODOLOGY

PLFD changes the original pattern shape to a shape that consists of many vertexes and minute edges. The complicated shape produced by PLFD causes a decrease in exposure throughput because it increases the number of exposure shots for EBL, and makes the precision deteriorate because of exposing them using minute beams. However, these obstacles and faults can be resolved by using an e-beam cell projection (CP) exposure method [7, 8, 9]. An increase in the number of shots and the requirement of high resolution can be satisfied by using CP cells in Fig. 3. In other words, a high throughput and high resolution can be maintained for PLFD patterns, because all patterns on a CP-cell are reduced to 1/60 from 1/25 and are produced a shot at a time on a wafer as shown in Figs. 3(a), 3(b), and 3(c). In this paper, a CP-cell with PLFD patterns is called a PLFD CP-cell.

3.1 Applying PLFD by using an electron beam cell projection exposure method

There are difficulties in realizing a PLFD CP-cell of a complicated shape. One of the difficulties is the load on the computational processing to generate e-beam exposure data from the tape-out data of a chip. We solve this problem by replacing the CP-cells of the exposure data with the PLFD CP-cells after making e-beam exposure data from the original tape-out data. This is the most effective way of saving on computer resources and calculation time. Moreover, another

difficulty is the load on the formation conditions on a PLFD-cell. One CP-cell includes patterns of different shapes, and those patterns are given the same exposure dose. We have been adopting the proximity effect correction (PEC) which the pattern shape modification for the forward scattering and the dose correction for the back scattering are separately applied [10]. We are able to overcome this CP-cell issue by modifying the shape in consideration of the forward scattering effects in PLFD in Fig. 4(a). Furthermore, we must permit the limit of CP mask fabrication. Therefore, we define PLFD criteria as the **difference** from photolithography images in Fig. 5(a), the **edge length** for CP mask fabrication in Fig. 5(b), and **exposure area difference** with original CP-cell for PEC in Fig. 5(c). PLFD is required to satisfy these three items as shown in Fig. 5.

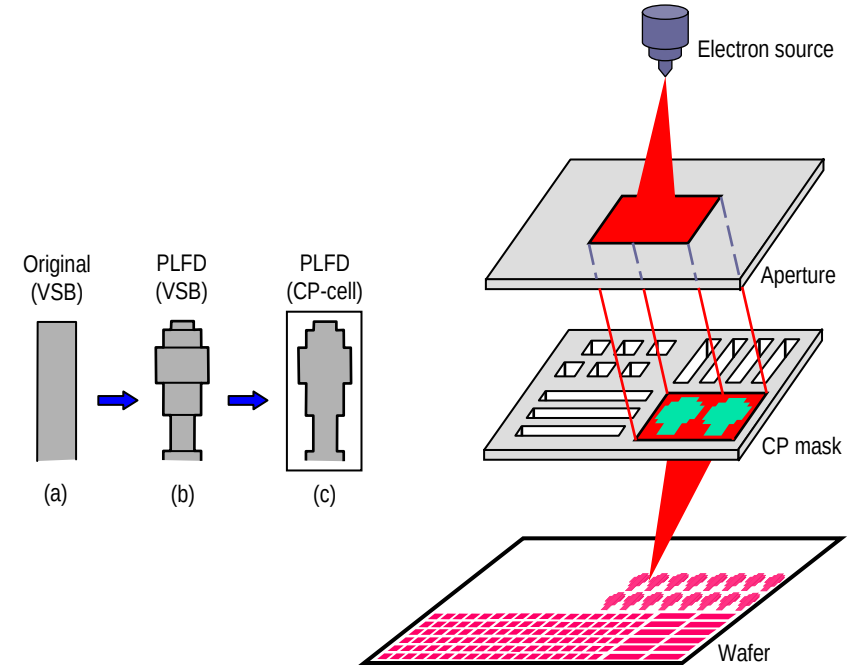

Fig. 3. Schematic representation of an e-beam cell projection (CP) exposure method. (a) The shot count of this original pattern is one with various shaped beam (VSB). (b) The shot count of the PLFD pattern is 6 with VSB. (c) The shot count of the PLFD pattern is one with CP.

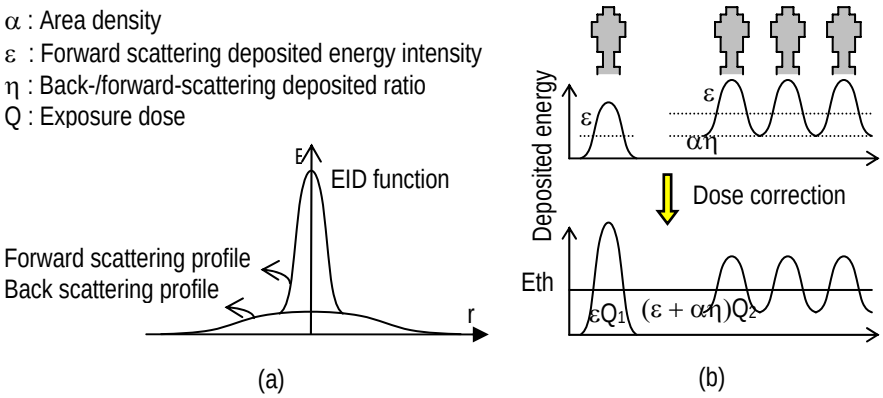

Fig. 4. Schematic diagram of the correction concept for PLFD. (a) The forward scattering effects are corrected using pattern shape modification; and the backscattering effects, using dose correction. (b) The backscattering effects to a PLFD CP-cell are corrected with its dose correction only.

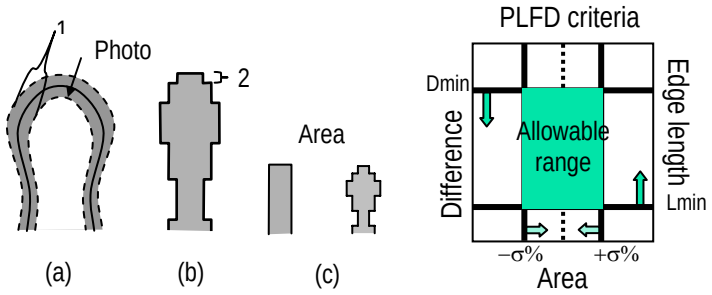

Fig. 5. Criteria for applying PLFD CP-cells and the allowable range: (a) The difference from photo image is labeled “1”; (b) The edge length is labeled “2”; (c) The irradiate area difference in a PLFD CP-cell and the original CP-cell.

3.2 Data processing system for applying PLFD

The conventional exposure data processing flowchart for CP e-beam exposure consists of two parts, as shown in Fig. 6(a). One, shown in the upper part of Fig. 6(a), makes a CP-cell library. The other one in Fig. 6(a) extracts CP-cell patterns from tape-out design data, converts the tape-out design data to e-beam exposure data, and gives the optimum exposure dose to correct the proximity effects for each exposure pattern. In the former process, this is executed whenever a design rule is defined. First, it selects the optimum common CP-cell patterns based on the design rule, the unit cell library, and the information in the Placing and Routing (P&R) phase. After that, it changes the CP-cell patterns by bias, extension or reform if necessary because accuracy is high. In the latter process, this is executed whenever the design data for manufacturing purposes is input.

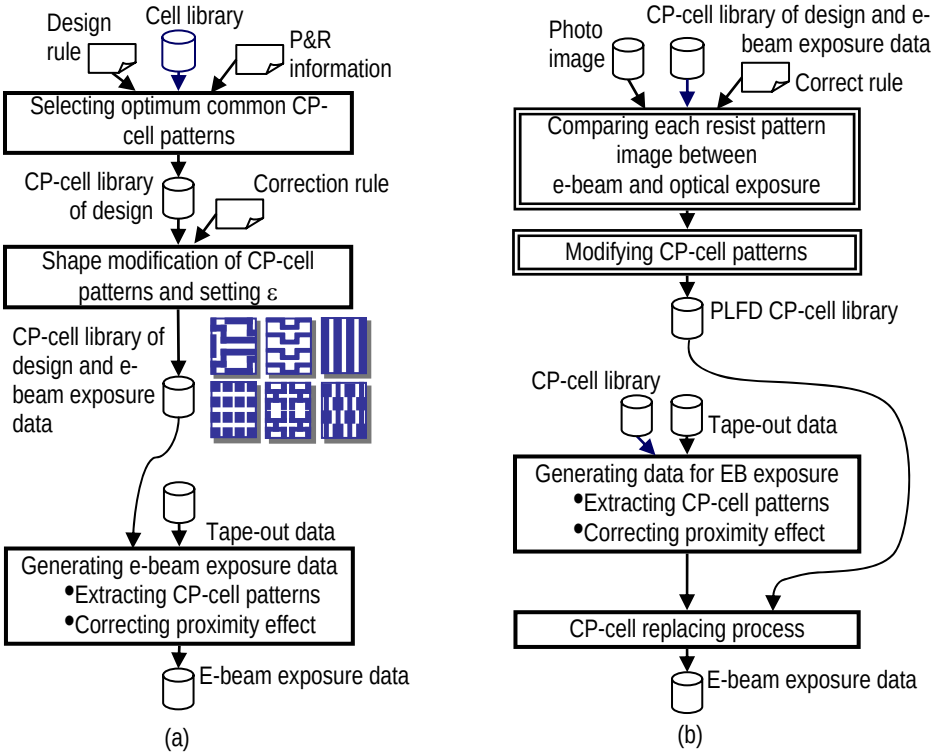

Fig. 6. Data processing flowcharts: (a) the conventional flowchart for CP exposure data; (b) the new flowchart for applying PLFD CP exposure data.

Figure 6(b) shows the flowchart of the exposure data processing to apply PLFD. Prior processing prepares a PLFD CP-cell library corresponding to each of CP-cell library. In generating e-beam exposure data, it replaces each CP-cell with the corresponding PLFD CP-cell in the PLFD CP-cell library after converting the original tape-out design data into e-beam exposure data. In the former process, this is executed whenever the CP-cell library is defined. First, it calculates the shape of the resist patterns of a CP-cell by EBL simulation. Second, it analyzes the different shapes in EBL and photolithography. After that, it modifies the original CP-cell patterns by using information about those different shapes. The generating flowchart of a PLFD CP-cell is shown in the next drawing.

3.3 Creating a PLFD CP-cell library for electron beam exposure

The flowchart for the procedure of creating a PLFD CP-cell for EBL is shown in Fig. 7. This process creates a PLFD CP-cell library for EBL. Faithful photolithographic image data, obtained from SEM or lithography simulation, of the CP-cell pattern is prepared beforehand.

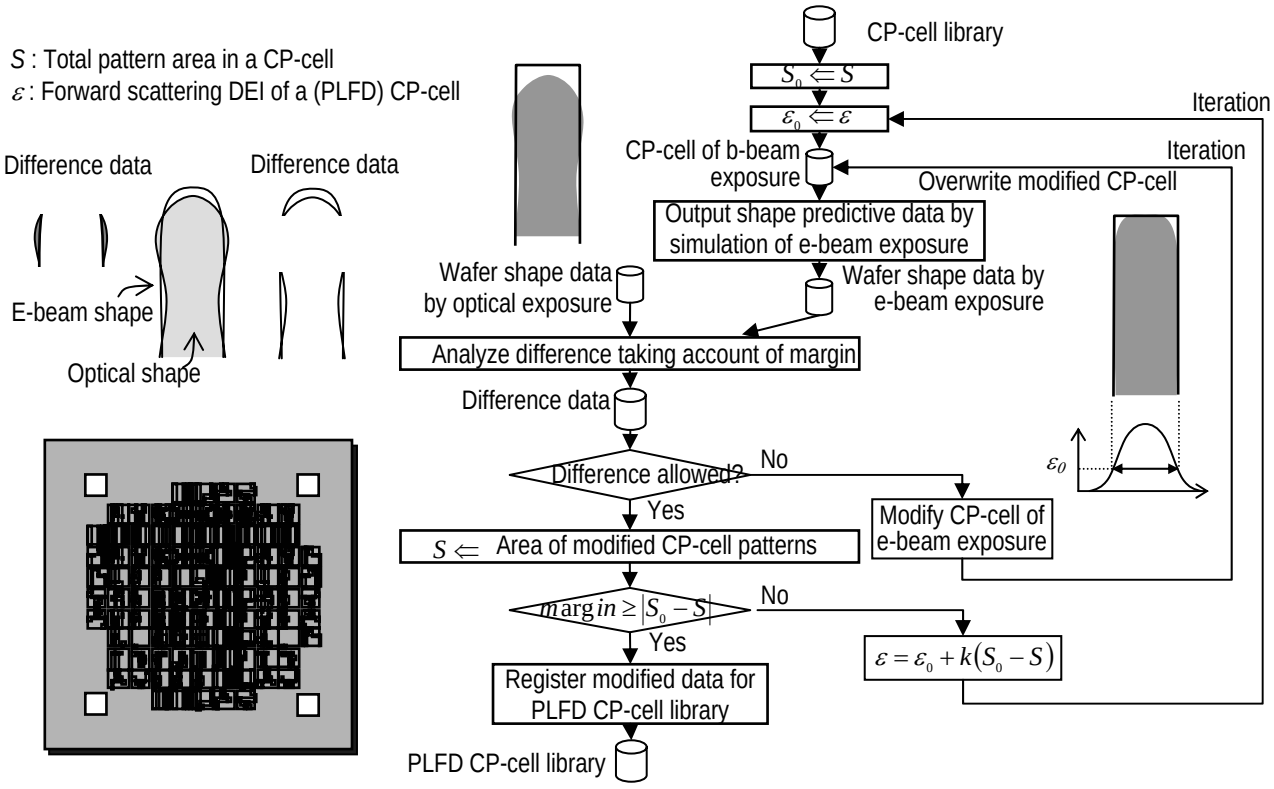

Fig. 7. Flowchart of the process creation PLFD CP-cell library for the e-beam exposure.

S is the total area of the patterns in a CP-cell. ε is the energy intensity where the width of the forward scattering energy intensity distribution (EID) obtains the aim width. First, S of a CP-cell pattern and ε of the CP-cell are substituted into S_0 and ε_0, respectively. The CP-cell patterns are modified as follows. First, with respect to the CP-cell, the patterns are converted into contour data of ε_0 by using the EID function based on EBL, and thus EBL images are output on the semiconductor substrate. Second, respective pieces of shape data are compared with this contour shape and photo images, thereby extracting a difference pattern. Next, it is judged whether or not this difference exceeds the allowable value. The CP-cell patterns are then modified using data about the difference patterns. This processing is repeated until the difference falls below the allowable value. Moreover, the area of a modified CP-cell pattern is compared with S_0, and it is judged whether or not the difference exceeds the allowable value. If the difference of the area exceeds the allowable value, ε is coordinated and the first processing is then re-applied.

4. RESULTS AND DISCUSSION

We applied the PLFD technique to actual 65-nm SRAM cell layouts. Because SRAM have high repeatability, they are exposed by the CP method to shorten the writing time. In addition, SRAM is one of the cells that are the most sensitive to device characteristics. Therefore, we investigate whether the PLFD technique can be effectively used for a CP-cell pattern design. The target layers are Diffusion, Poly, Contact, and Metal 1. EBL simulations were performed for a lithographic system using an e-beam source with an accelerating voltage of 50 kV. Photolithography simulations were performed for a lithographic system using an ArF light source with wavelength of 193 nm and the numerical aperture of 0.85.

4.1 Definition of the evaluation conditions

In subsection **3.3**, we have already defined three criteria of PLFD. In this investigation, we determine each item of the criteria as follows. The difference from the photo images is less than 2 nm which is a value that is less than the demanded precision of 5% for a 65-nm node. The minimum edge length is 1 nm on wafer which is the CP mask fabrication limit. The irradiate area difference with the original CP-cell is less than 0.1%. This value is derived from the change in area which is satisfied with critical dimension (CD) accuracy. The corrected dose for each CP-cell is expressed as

$$Q = \frac{E_{th}}{\varepsilon + \alpha\eta}. \tag{1}$$

Here E_{th} is the threshold energy, ε is the forward scattering deposited energy intensity (DEI), where the profile gives the same width as the target linewidth, α is area density, and η is the deposit energy ratio of the backscattering and the forward-scattering. Likewise, the original CP-cell $(\varepsilon_1, \alpha_1, Q_1)$ and the PLFD CP-cell $(\varepsilon_2, \alpha_2, Q_2)$ are described as

$$(\varepsilon_1 + \alpha_1\eta)Q_1 = E_{th}, \tag{2}$$

$$(\varepsilon_2 + \alpha_2\eta)Q_2 = E_{th}. \tag{3}$$

Because the PLFD CP-cell is actually exposed in dose Q_1 against the most suitable dose Q_2, a dose difference of $1 - \frac{Q_1}{Q_2}$ does emerge for CD variation. From Eqs. (2) and (3),

$$\frac{Q_1}{Q_2} = \frac{\varepsilon_2 + \alpha_2\eta}{\varepsilon_1 + \alpha_1\eta}. \tag{4}$$

CD variation ΔW is written as

$$\Delta W = \Delta W_0\left(\frac{Q_1}{Q_2} - 1\right) = \Delta W_0\left(\frac{\varepsilon_2 + \alpha_2\eta}{\varepsilon_1 + \alpha_1\eta} - 1\right), \tag{5}$$

where ΔW_0 is the variation of CD with the change of the dose per unit. We express this area density in area S in unit domain S_0. After substituting $\alpha_1 = \frac{S_1}{S_0}$, $\alpha_2 = \frac{S_2}{S_0}$, and $\Delta S = S_2 - S_1$ into Eq. (5) and rearranging the terms we obtain

$$\Delta W = \Delta W_0 \left(\frac{\varepsilon_2 S_0 + (S_1 + \Delta S)\eta}{\varepsilon_1 S_0 + S_1 \eta} - 1 \right), \tag{6}$$

where ΔS is the area variation of a PLFD CP-cell compared with the original CP-cell. Equation (6) is solved with ΔS ,

$$\Delta S = \left(\frac{\varepsilon_1}{\eta} S_0 + S_1 \right) \left(1 + \frac{\Delta W}{\Delta W_0} \right) - \left(\frac{\varepsilon_2}{\eta} S_0 + S_1 \right). \tag{7}$$

Therefore, the relation between ΔS and the maximum of the allowed CD variation $\Delta W_{\max}$ is obtained,

$$\Delta S \le \left(\frac{\varepsilon_1}{\eta} S_0 + S_1 \right) \left(1 + \frac{\Delta W_{\max}}{\Delta W_0} \right) - \left(\frac{\varepsilon_2}{\eta} S_0 + S_1 \right). \tag{8}$$

We define $\Delta W_{\max}$ of 65 nm in a SRAM cell as 0.5 nm and calculate ΔS from Eq. (8), then obtain the irradiate area difference.

4.2 Experimental results

The feasibility of the PLFD CP-cells in the 65-nm SRAM cell is confirmed regarding the three items in mentioned above. First, we show the investigation results of the difference from photo images with the contact layer as an example.

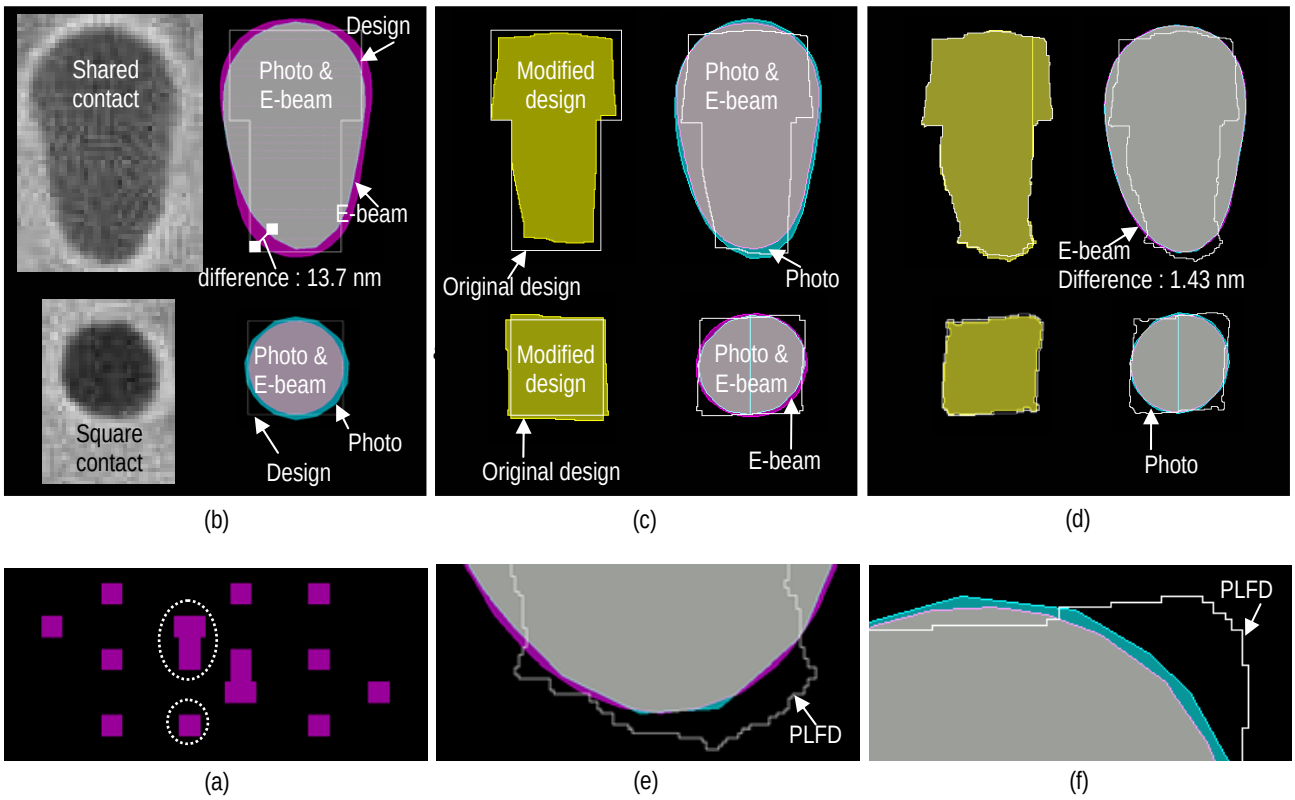

Fig. 8. PLFD results of contact patterns in 65-nm node scale SRAM cell: (a) the original CP-cell; (b) EBL resist pattern images of shared contact and square contact patterns, and those contour images by EBL and photolithography simulations; (c) first modified pattern results; (d) final modified pattern results (e) the enlarged picture at the bottom of the shared contact in (d); (f) the enlarged picture at the upper right of the square contact in (d).

Figure 8(a) is a CP-cell of the sample, and the inside patterns of the white dashed circle marks in figure 8(a) are explained in Fig 8(b) through 8(f). Figure 8(b) shows the resist pattern images of shared contact and square contact patterns represented in each exposure and the simulation results. As seen in the SEM images on the left of Fig. 8(b), these results are very consistent with the e-beam simulation result in the contour images on the right of Fig. 8(b). The results for shared and square contact patterns in the same CP-cell are shown in contour images of Figs. 8(c) and 8(d). The contour images on Fig. 8(b) illustrate the contour shapes, which are calculated by the e-beam lithographic simulator and the photolithographic simulator, on the contact layer in the original design data. They represent the patterns of the design data for comparison. The maximum difference in the contour shapes obtained from the EBL simulation and the photolithography simulation was 13.7 nm as shown in Fig. 8(b). The contour images in Figs. 8(c) and (d) show the first and the last modification results. In the case of this CP-cell, 4-times iterations achieved a CP-cell pattern design within 2-nm of the photolithography results as shown in Fig. 8(d). As can be seen in Figs 8(e) and 8(f), PLFD patterns become complicated shapes in corner parts of the original design especially.

Next, we show the investigation results of the edge length with the Metal 1 layer as an example. Figure 9(a) is an original CP-cell of the sample. We prepared four kinds of PLFD CP-cell designs in the contour grid size as shown in Figs. 9(b) through 9(e). The contour grid size means the grid size of the contour by the EBL simulation, and the modify grid size means the grid size of the modified pattern by PLFD technique. As a matter of course, the difference criterion is satisfied on all PLFD CP-cells. The upper pictures in these figures show PLFD CP-cells of each grid size. The patterns of the PLFD CP-cells are divided with a rectangle or a triangle. The middle SEM pictures in Fig. 9 show PLFD-generated CP mask, and the center of these SEM mask images are enlarged at the lower pictures in Figs 9(b) through 9(e). As can be seen from these figures, the difference criterion can be achieved even by a contour grid of 3.0 nm, and even a PLFD CP-cell with a contour grid of 0.1 nm can be fabricated perfectly.

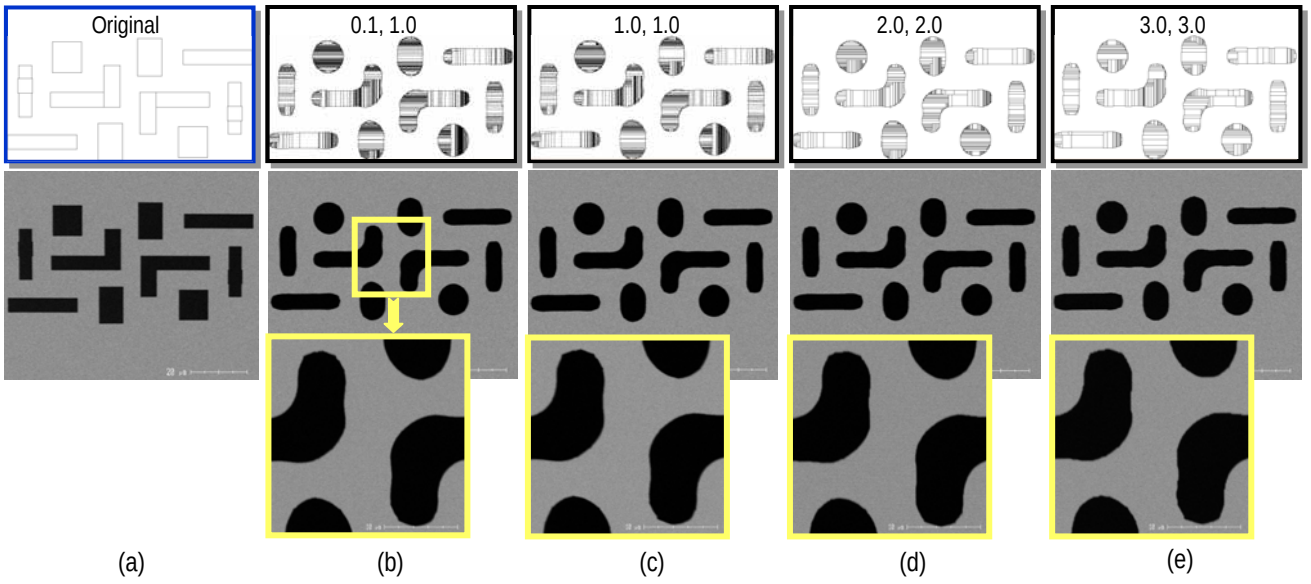

Fig. 9. Relationship between the contour grid size and CP mask: (a) the original CP-cell; (b) PLFD CP-cell by a contour grid size of 0.1 nm and a modify grid size of 1.0 nm; (c) PLFD CP-cell by the contour of 1.0 nm and the modify of 1.0 nm grid size; (d) PLFD CP-cell by 2.0 nm grid sizes respectively; (e) PLFD CP-cell by 3.0 nm grid sizes respectively.

Lastly, we show the investigation results of the irradiated area difference with the Poly layer as an example. The upper picture of Fig. 10(b) is an original CP-cell of the sample. We prepared likewise four kinds of PLFD CP-cell designs in the contour grid size as shown in Figs. 10(c) through 10(f). As a matter of course, the difference and edge length criteria are satisfied on all PLFD CP-cells, too. As can be seen from Table 1, these four PLFD CP-cells are designed with area differences within 0.1% of the original CP-cell. Furthermore, the validity of this criterion becomes more certain by

confirming the exposure dose. In other words, both doses between the exposure shot generated from the original CP-cell and that generated from PLFD CP-cell must be the same because the CP-cell in the original exposure data is replaced by the PLFD CP-cell. As shown in the geometry of Fig. 10(a), we arranged the CP-cell with isolation and array. The dimension of the array area is 12 um x 15 um, and each of the isolations is 10 um, 20 um, 30 um, and 40 um away from the corner of the array area respectively. We prepared for data arranged in this way from an original CP-cell and each PLFD CP-cell. These two sets of data were converted into the e-beam exposure data with the same PEC conditions. The dose ratio values in the original CP-cell data were that "Array" ranged from 2.498 to 2.688, "Iso1" was 2.989, and from "Iso2" to "Iso4" were 3.005. The dose maps on Figs. 10(b) through 10(f) show the dose values with color. The dose ratio values of the PLFD CP-cell data can be confirmed as being the same as those in the original CP-cell data. We were able to confirm that the dose values of the PLFD CP-cell data were consistent with those of the original CP-cell data.

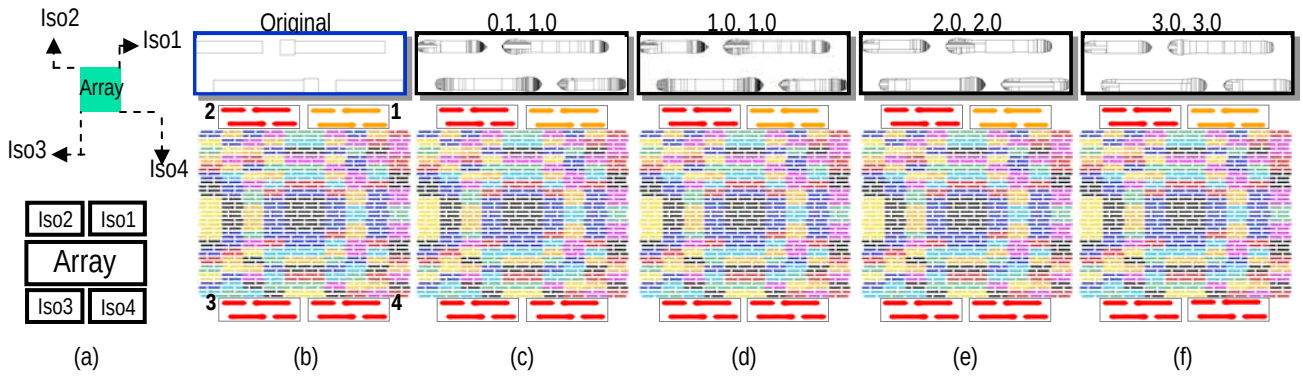

Fig. 10. Relationship between the contour grid size and the exposure dose: (a) geometry of CP-cell; (b) original CP-cell; (c) PLFD CP-cell by 0.1 nm contour grid and 1.0 nm modify grid; (d) PLFD CP-cell by 1.0 nm grid size; (e) PLFD CP-cell by 2.0 nm grid size; (f) PLFD CP-cell by 3.0 nm grid size.

4.3 Mask manufacturing and wafer exposure by the PLFD CP mask

We manufactured a PLFD CP mask. In the range of the grid size that we prepared for, the production of PLFD CP-cells did not appear any problems, as can be seen from Figs. 9, 11(c), and 12. Moreover, we exposed a wafer using this PLFD CP mask. The CP exposure tool that we used is from ADVANTEST's F-series. They are 50-keV tools for application with a maximum of 100 CP cells and a CP-cell size of 5 um.

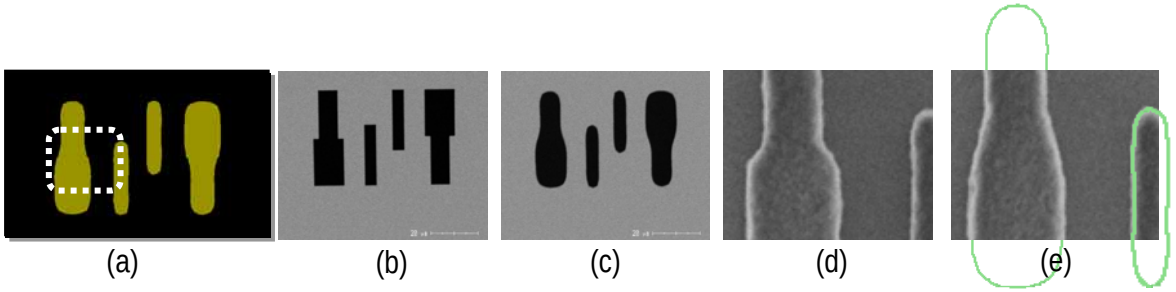

Fig. 11. SEM images on mask and on wafer: (a) the PLFD CP-cell data by the 0.1 nm contour grid size; (b) the original CP-cell on mask; (c) (a) on mask; (d) a portion on wafer exposed with (b); (e) a portion of the square in (a) on wafer, and is overlaid with the target contour of the photolithography.

We show the exposure results with the Diffusion layer in Fig 11. Both SEM images in Figs. 11(d) and 11(e) were exposed with the same dose on the wafer. There is the remarkable difference in shape between the original CP-cell and the PLFD CP-cell as shown in Figs. 11(d) and 11(e). The resist pattern on the wafer can observe that the PLFD result in Fig. 11(e) conforms with the contour target very well. Furthermore, Fig. 12 shows the difference in the grid size with the Poly layer. These PLFD CP-cells were exposed with the same dose on the wafer. The width of the target contour at the measurement point as shown in Fig 12(b) was 106.8 nm. Each width of the same point in Figs. 12(c) through 12(f) was 106.3 nm, 107.4 nm, 107.4 nm, and 106.4 nm respectively. Typical grid size trends were not indicated, and the resist pattern by the PLFD CP-cell as shown in Fig. 12(f) conforms with the contour target very well. All PLFD CP-cells produced good results.

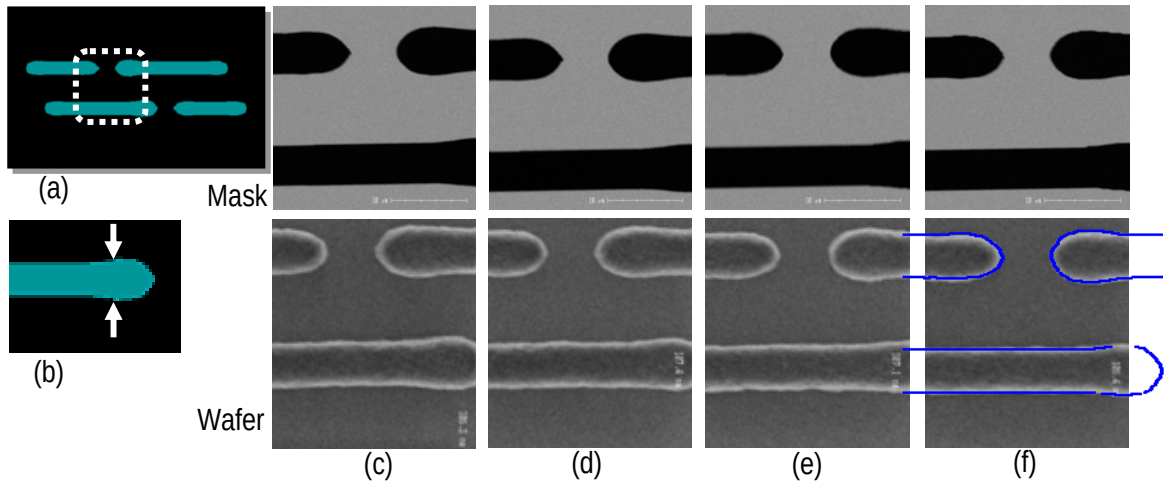

Fig. 12. Dependence on the grid size: (a) the PLFD CP-cell data by the 0.1 nm contour grid size; (b) the measurement point; (c) SEM images on mask and on wafer by the 0.1 nm contour grid; (d) SEM images on mask and on wafer by the 1.0 nm contour grid; (e) SEM images on mask and on wafer by the 2.0 nm contour grid; (f) SEM images on mask and on wafer by the 1.0 nm contour grid, and is overlaid with the target contour of the photolithography.

Table 1. All evaluation results.

Layer (Number of fractions of Original)	Edge length [nm] (Contour grid)	Difference [nm]	Number of fractions (PLFD / Original)	Area [%]
Diffusion (6)	1.0 (0.1)	1.5	1405 (234.17)	99.98654
	1.0 (1.0)	1.6	1004 (167.33)	99.99113
	2.0 (2.0)	1.7	629 (104.83)	99.95044
	3.0 (3.0)	1.8	441 (73.50)	99.90002
Poly (8)	1.0 (0.1)	0.8	1334 (222.33)	100.06280
	1.0 (1.0)	1.0	812 (136.33)	100.06690
	2.0 (2.0)	1.2	503 (83.83)	99.92887
	3.0 (3.0)	1.4	340 (56.67)	100.05910
Contact (14)	1.0 (0.1)	1.0	2218 (158.43)	99.96827
	1.0 (1.0)	1.3	1513 (108.07)	99.98308
	2.0 (2.0)	1.6	886 (63.29)	99.96156
	3.0 (3.0)	1.8	625 (44.64)	99.90007
Metal 1 (16)	1.0 (0.1)	1.2	3060 (191.25)	100.00050
	1.0 (1.0)	1.3	2147 (134.19)	100.00510
	2.0 (2.0)	1.6	1349 (84.31)	100.00320
	3.0 (3.0)	1.7	920 (57.50)	99.90002

Table 1 summarizes the results of all the PLFD CP-cells. The number of fractions on the table means the number of partitions when the pattern of the PLFD CP-cell is divided with a rectangle or a triangle. In all data in the evaluation object, we were able to design a PLFD CP-cell which satisfied the criteria. Moreover, it was experimentally proven that these PLFD CP-cells were fabricated on a CP mask surely, and the exposing a wafer with these makes could faithfully form resist patterns. According to this PLFD CP-cell library for EBL, the shape equal to the shape produced when using photolithography can be obtained using e-beam exposure.

5. CONCLUSIONS

In this paper, we have demonstrated applications of a photolithography-friendly design (PLFD) technique for 65-nm semiconductor node using an actual product layout at SRAM cell production fabrication facilities. Moreover, we revealed our implementation method for a PLFD technique. Thus, even if the resist on the semiconductor substrate is exposed to electron beams, we showed that the same resist shape as the one produced in optical exposure can be acquired. This PLFD technique can be very effectively used in the semiconductor device business. In our explanation and demonstration, this method was described by exemplifying the optical exposure technology and the electron beam exposure technology and it can also be applied to combinations of other types of technologies.

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