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SILICON RESULTS VALIDATE DESIGN FOR E-BEAM METHODOLOGY AT THE 65-NM NODE

D2S, e-Shuttle and Fujitsu Microelectronics Collaborate On First Test Chip

SAN JOSE, Calif., May 26, 2009—The eBeam Initiative, a forum dedicated to the education and promotion of a new design-to-manufacturing approach known as design for e-beam (DFEB), today announced that steering group members D2S, Inc., e-Shuttle, Inc. and Fujitsu Microelectronics Limited have validated the DFEB methodology for low-volume, 65-nm system-on-chip applications, without sacrificing performance, area or power. DFEB combines software and design technologies that enable today's most advanced character projection (CP) e-beam direct-write (EbDW) equipment to reduce shot count, thus making EbDW throughput feasible for low-volume designs. Today's announcement marks a significant milestone as it demonstrates early progress on the three-year roadmap.

The final estimated shot count for the test chip using DFEB represented a more than 10X reduction over conventional EbDW technologies, while also meeting the required performance, power and area goals. The collaborative effort drew from a number of companies involved in the eBeam Initiative. Specifically, D2S and Fujitsu Microelectronics worked on the design while e-Shuttle manufactured the test chip to confirm the DFEB technology for the 65-nm node. D2S designed the DFEB library overlay with Fujitsu Microelectronics and also partnered closely with e-Shuttle and Advantest Corporation on the stencil mask used in the fab's EbDW machine. Prototyping is a target application for DFEB, and with e-Shuttle's experience in these services, they were able to validate the applicability of DFEB for prototyping.

According to Yoji Hino, corporate executive vice president of Fujitsu Microelectronics Limited and member of the eBeam Initiative steering group, "With this test chip, we now have tangible results that DFEB is enabling us to meet the necessary shot count requirements without sacrificing the quality of design results. DFEB makes maskless prototypes practical now."

A related paper jointly authored by Advantest, D2S, e-Shuttle and Fujitsu Microelectronics Limited will be presented by e-Shuttle at the session of Electron Beam Lithography Tools during the 53rd International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication (EIPBN), taking place May 26-29 in Marco Island, Fla. The article, titled "DFEB, a novel approach to EbDW throughput enhancement for volume production," will be available online after May 29 at www.ebeam.org.

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A presentation about the DFEB design methodology used for the test chip by eBeam Initiative members D2S, Fastrack Design and Magma Design Automation can also be found at this website. D2S and Fastrack Design implemented the test chip design using Talus® software from Magma®.

About The eBeam Initiative

The eBeam Initiative provides a forum for educational and promotional activities regarding a new design-to-manufacturing approach, known as design for e-beam (DFEB). DFEB reduces mask costs for semiconductor devices by combining design, design software, manufacturing, manufacturing equipment and manufacturing software expertise. The goals of the Initiative are to reduce the barriers to adoption to enable more integrated circuit (IC) design starts and faster time-to-market while increasing the investment in DFEB throughout the semiconductor ecosystem. Members, advisors and the steering group, which span the semiconductor ecosystem, include: Advantest, Alchip Technologies, Altos Design Automation, Cadence Design Systems, CEA/Leti, D2S, Dai Nippon Printing, D. E. Shaw Research, e-Shuttle, eSilicon Corporation, Fastrack Design, Fujitsu Microelectronics, Magma Design Automation, PMC-Sierra, Qualcomm, STMicroelectronics, Tela Innovations, Toppan Printing, Virage Logic and Vistec Electron Beam Lithography Group. Membership is open to all companies and institutions throughout the electronics industry. To find out more, please visit www.ebeam.org.

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