IMS Nanofabrication *member of* eBeam Initiative

Printing results from a multi-beam mask exposure tool

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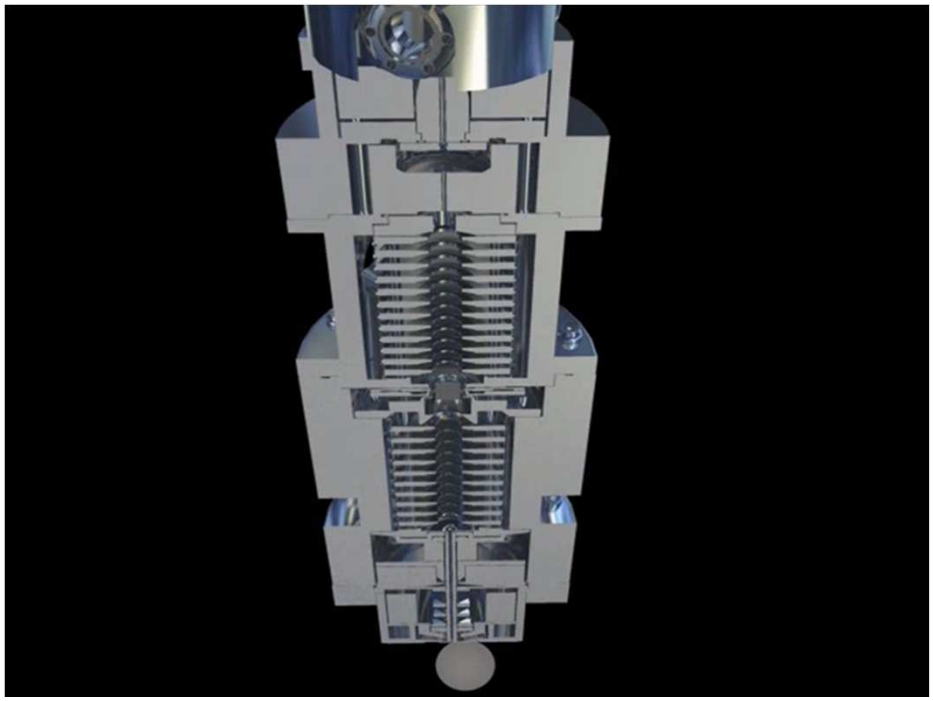
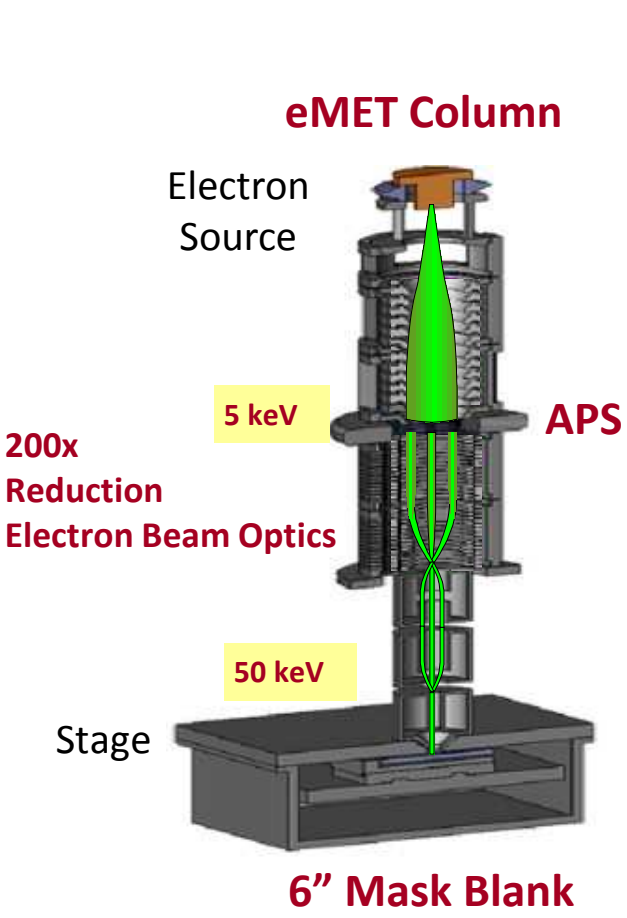
Sept 11, 2012, Monterey Marriott

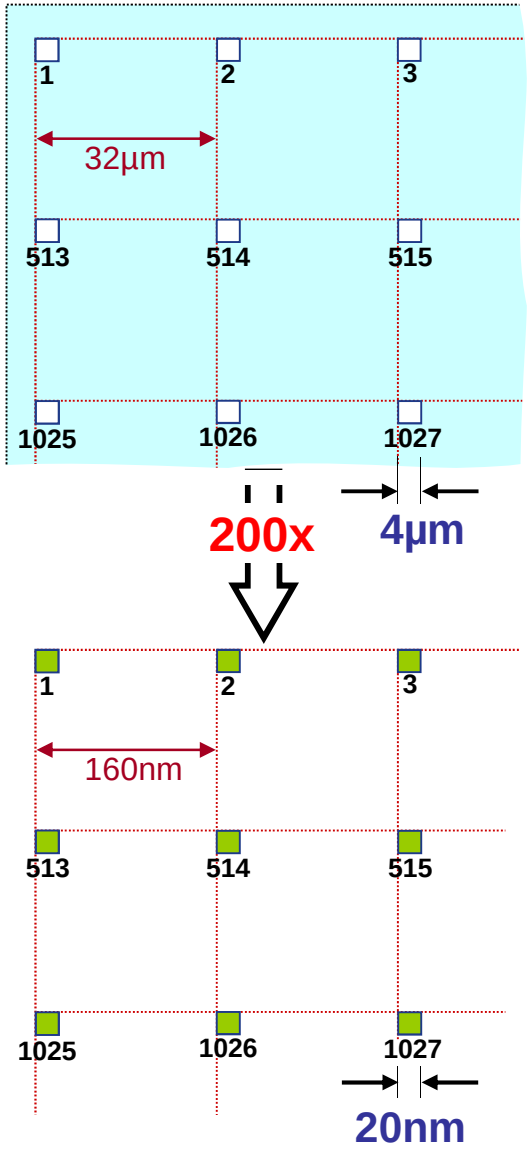
eMET POC



- Column designed for 11nm HP (8nm logic) node
- Column extendibility to 8nm HP and 6nm HP nodes

eMET Column with 262,144 programmable beams





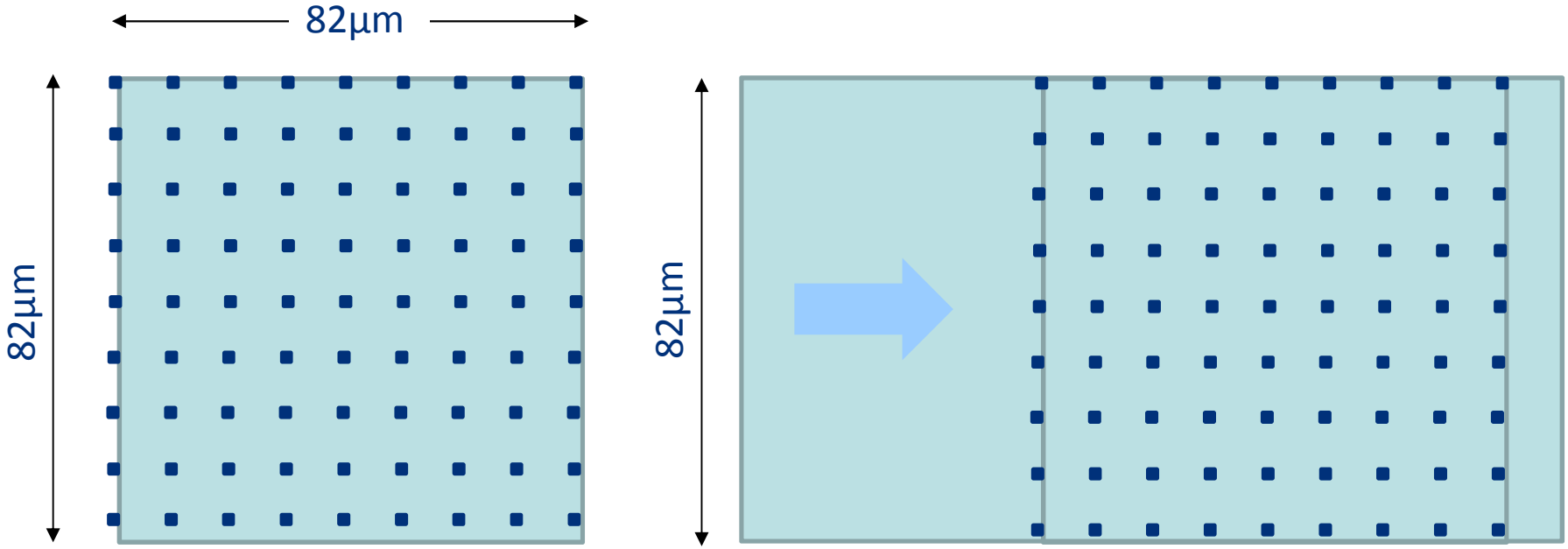
at APS (Aperture Plate System)

Aperture	4µm x 4µm
Cell Size	32µm x 32µm
# Cells	512 x 512
# Apertures	262,144

at 6“ Mask Blank

Beam Size	20nm x 20nm
Cell Size	160nm x 160nm
# Cells	512 x 512
# Beams	262,144

Stationary Stage & Scanning Stripe Multi-Beam Exposure



Stationary Stage Write Mode

Beam array deflected by multipoles

Purpose: debugging, calibration

Exposure of 82µm square region

Scanning Stripe Write Mode

Beam array deflected ±160nm

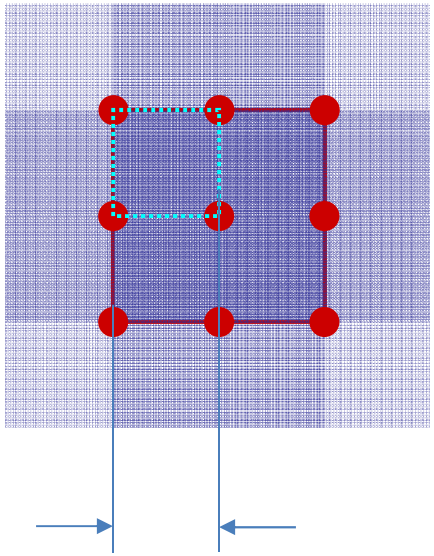
Stage at constant velocity

Exposure of 82µm wide stripes

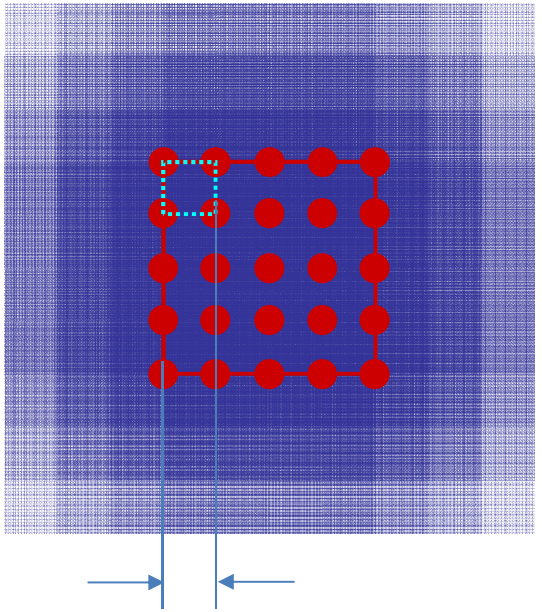
MESA

Multiple Exposure Shot Addressing

DOUBLE Grid



Pixel Size = ½ Beam Size



QUAD Grid

Pixel Size = ¼ Beam Size

Each spot exposed with 4bit: 16 dose levels (0, 1, 2, ….15)

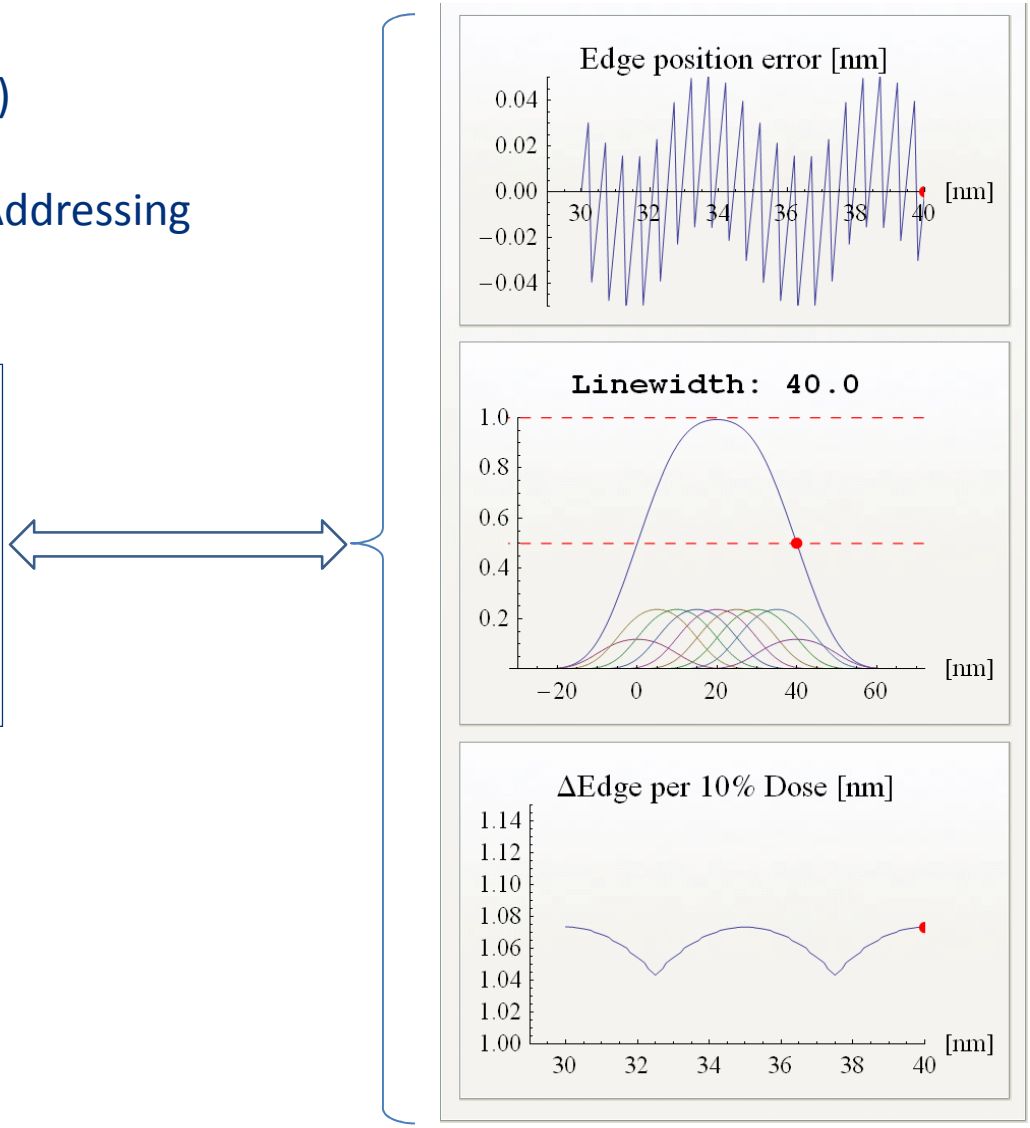
MESA with QUAD Grid

- Every 20nm shot exposed with
  4bit = 16 dose levels (0, 1, 2,….15)

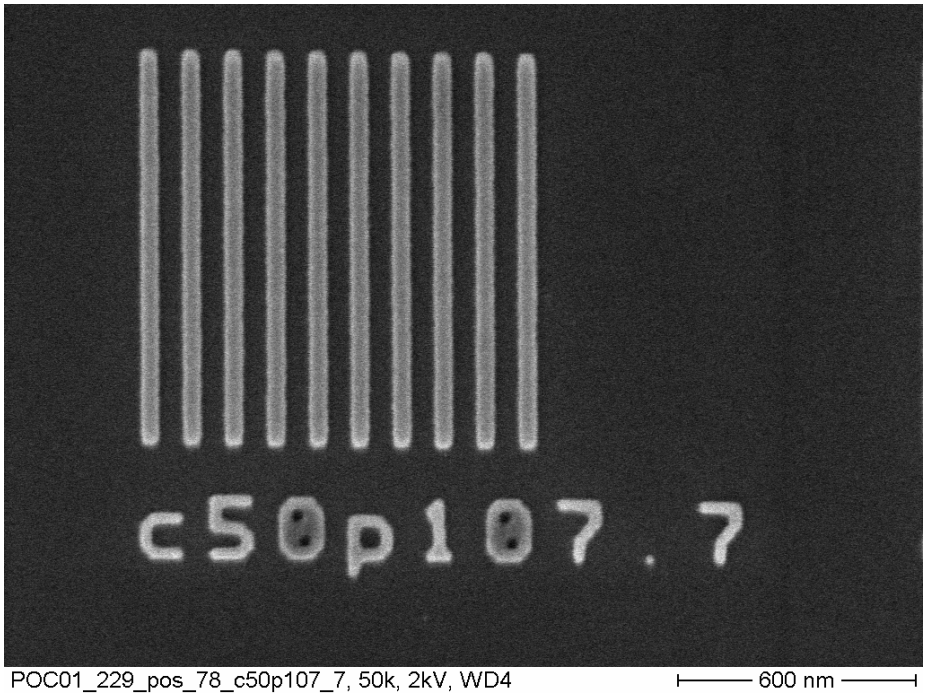
- **MESA –** Multiple Exposure Shot Addressing

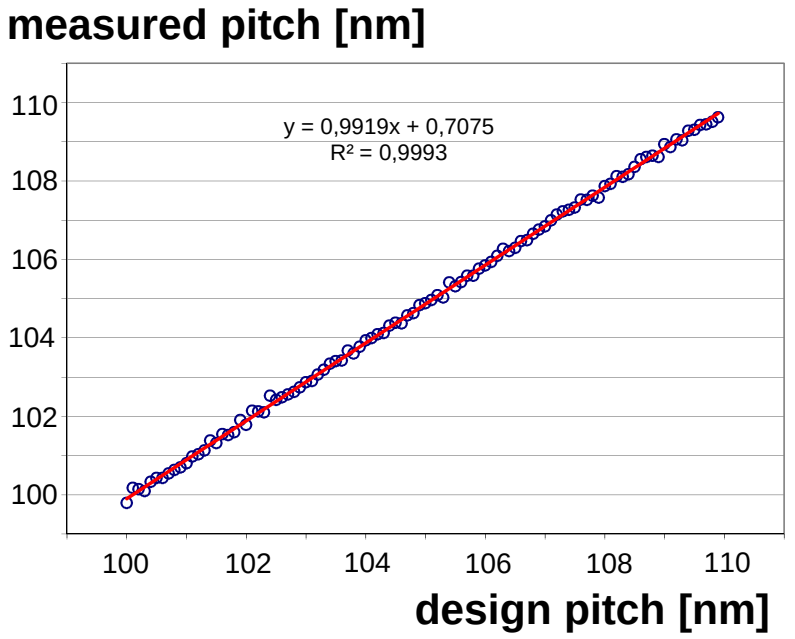
QUAD Grid:

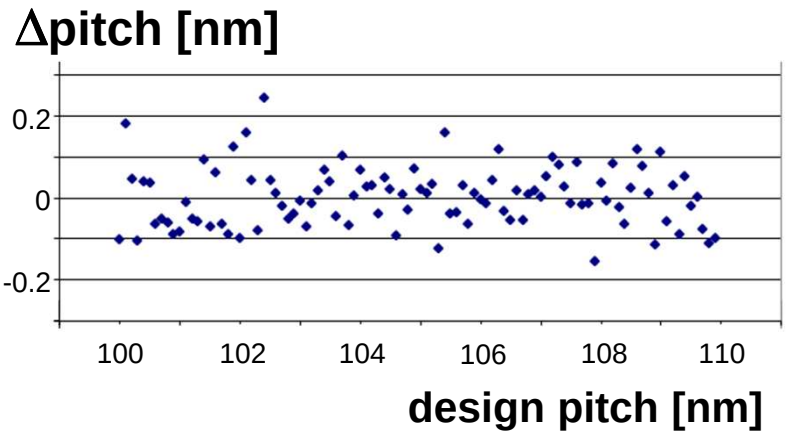
Beam Size: 20 nm
Pixel Size: 5 nm
⇨
16 x 15 + 1: 241 dose levels / area
4 x 15 + 1: 61 dose levels / edge



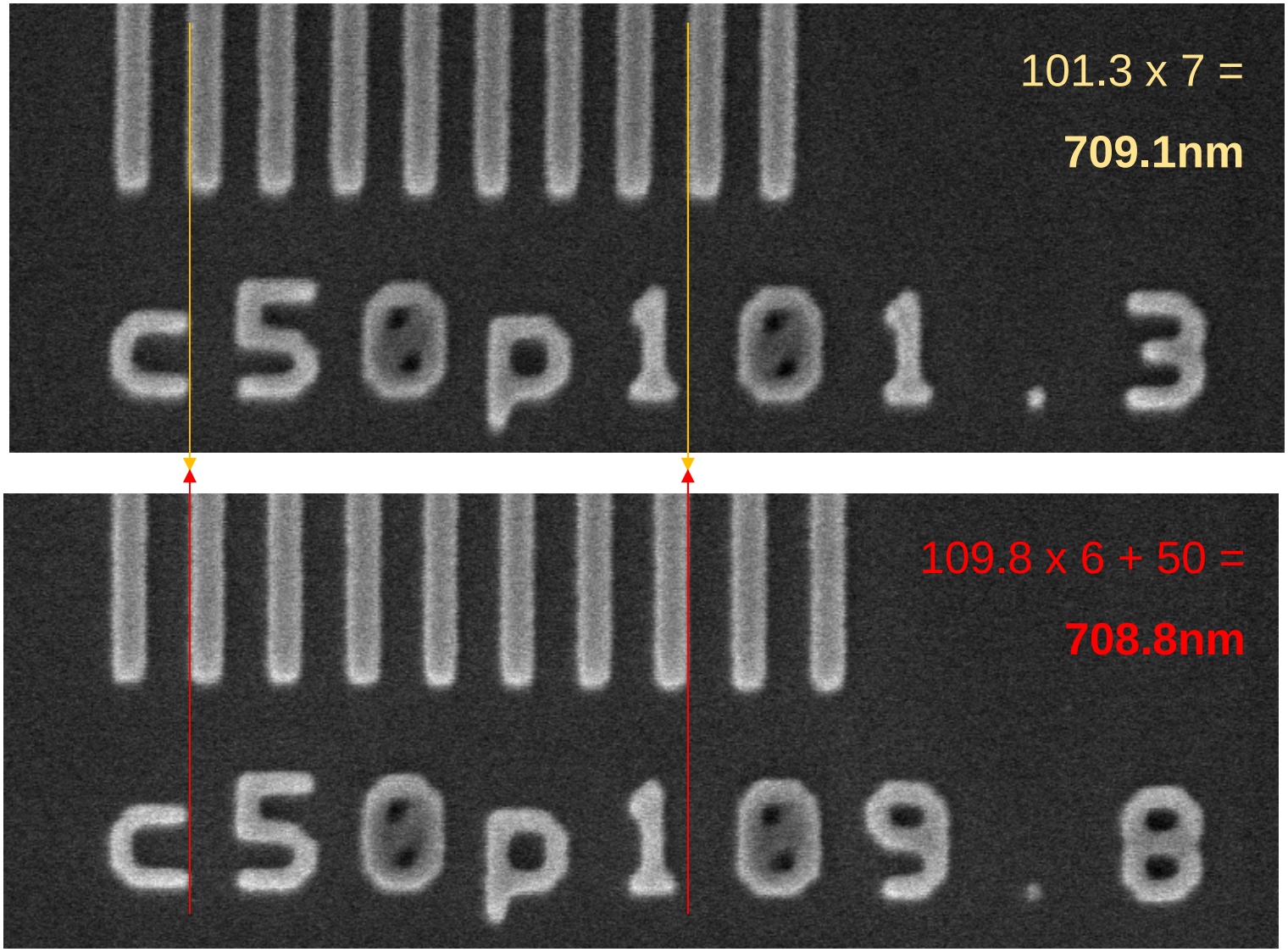
Multi-Beam Writing with 0.1nm Address Grid







Multi-Beam Writing with 0.1nm Address Grid

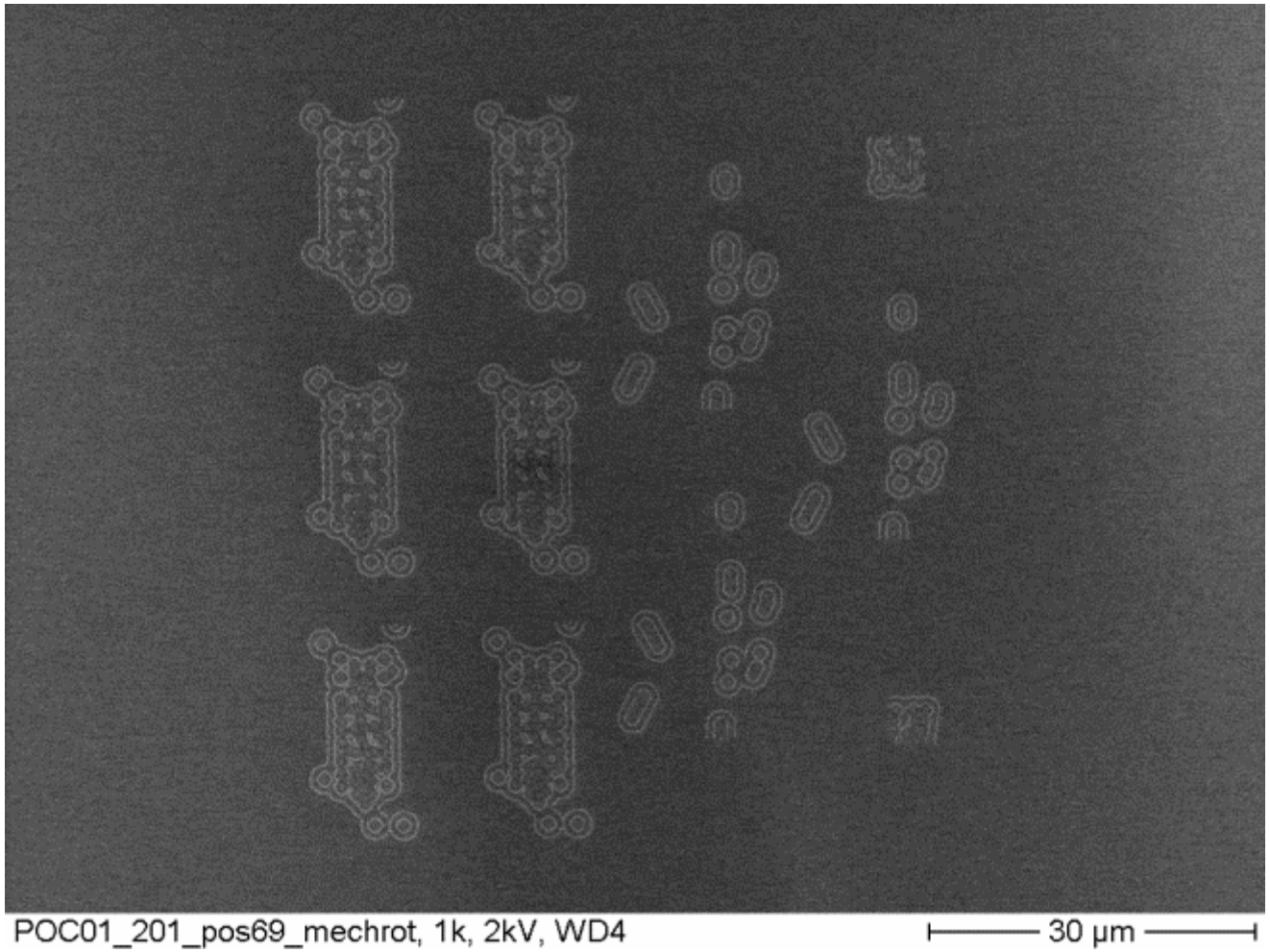


eMET POC exposure with 256k-APS ILT device test pattern

ILT device
test pattern

Design: DNP

Scanning Stripe exposure	20nm beam size	5nm pixel size	with PEC



eMET POC exposure with 256k-APS ILT device test pattern

ILT device
test pattern

Design: DNP

Scanning Stripe exposure	20nm beam size	5nm pixel size	with PEC

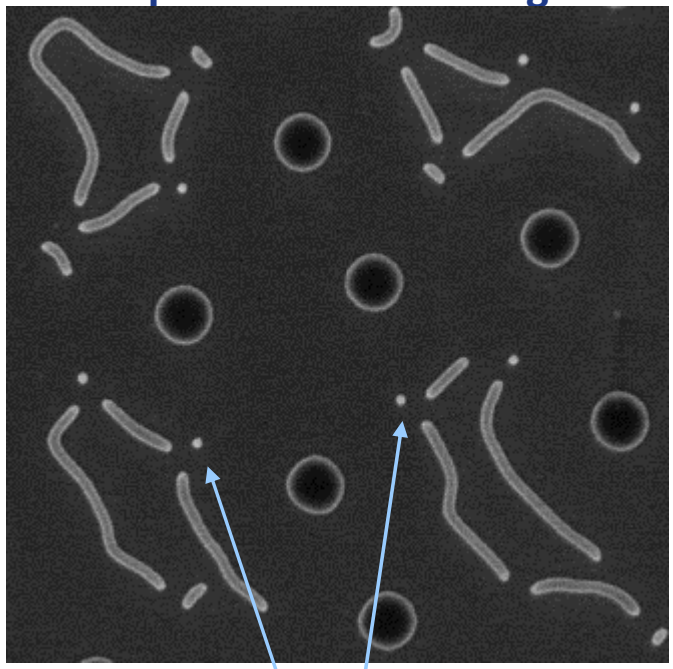
eMET POC exposure with 256k-APS ILT device test pattern

ILT device
test pattern

Design: DNP

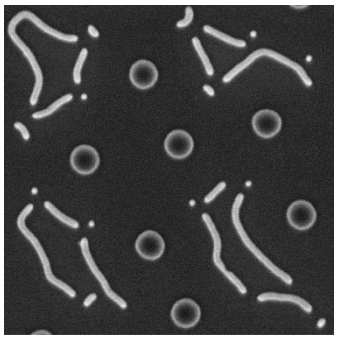
Scanning Stripe exposure	20nm beam size	5nm pixel size	with PEC

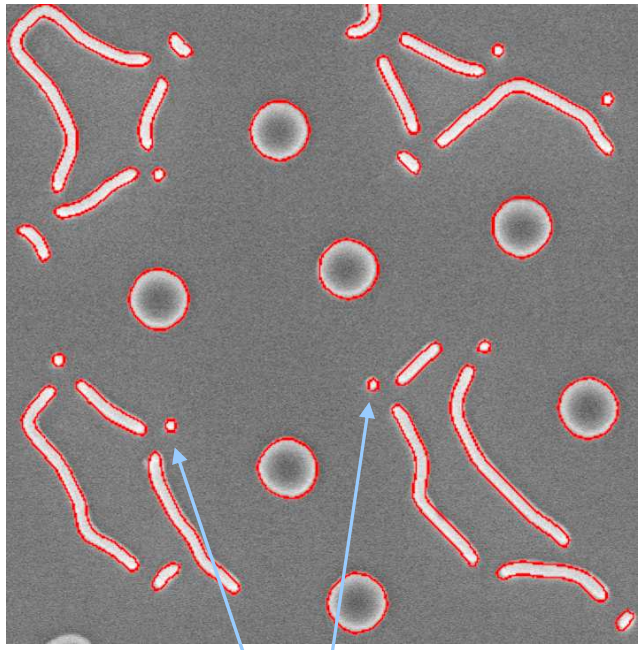
exposure of DNP design



60nm dots

exposure 2-times smaller





Design

30nm dots

eMET Schedule

	POC	ALPHA	BETA	1st gen. HVM
	2012	**2014**	**2015**	**2016**
Technology Node	Test: 11nm HP (8nm Logic)	11nm HP (8nm Logic)	11nm HP (8nm Logic)	11nm HP (8nm Logic)
Data Path & APS Speed	12.8 Gbits/s	12.8 Gbits/s	120 Gbits/s	120 Gbits/s
Beam Array Field	82µm x 82µm	82µm x 82µm	82µm x 82µm	82µm x 82µm
max Current Density	1 A/cm^2	1 A/cm^2	1 - 4 A/cm^2	1 - 4 A/cm^2
# Beams (k=1024)	256k	256k	256k	256k
Beam Size	20nm	20nm	20nm - 10nm	20nm - 10nm
max Current (all beams "on")	1 µA	1 µA	1 µA	1 µA
Throughput (≥ 100µC/cm^2)	10 cm^2/h	15h / mask	10h / mask	10h / mask

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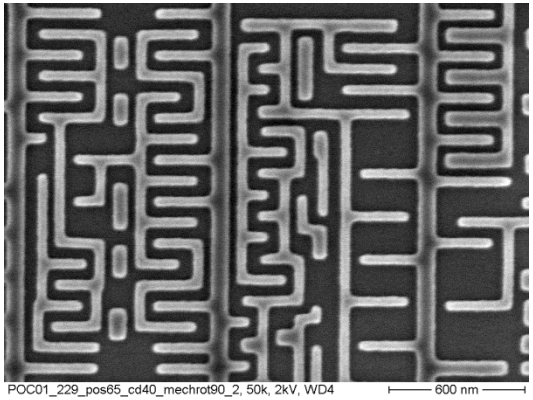
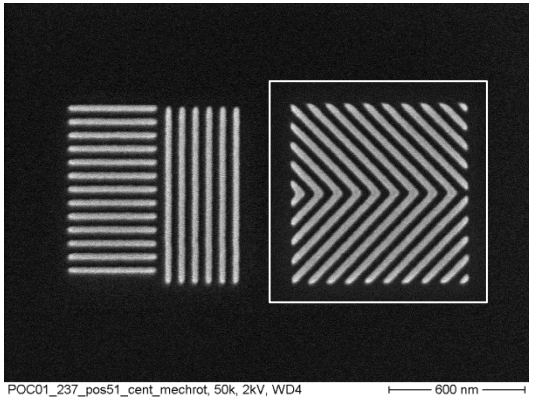
Thank You for Your Attention !

Synopsys - IMS poster presentation
Tuesday, 6:00pm - 7:30pm
[8522-87]

40nm HP
Metal



IMS oral presentation
Thursday, Session 12, 11:00am - 11:20am
[8522-52]



30nm HP
0°,45°,90° L&S