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**20 ELECTRONICS INDUSTRY LEADERS COLLABORATE TO ACCELERATE
DEVELOPMENT AND ADOPTION OF DESIGN FOR E-BEAM TECHNOLOGY**

***eBeam Initiative Aims to Increase Design Starts and
Reduce Time-to-market in Semiconductor Industry***

SAN JOSE, CALIF., February 24, 2009—A group of leading companies throughout the electronics industry today announced the launch of the eBeam Initiative—a forum dedicated to the education and promotion of an innovative, new design-to-manufacturing approach known as design for e-beam (DFEB). By enabling a decrease in mask costs for semiconductor devices, DFEB is expected to ultimately result in an increased number of design starts and reduced time-to-market for a wide range of semiconductor devices.

Charter members in the new initiative, which span the entire semiconductor ecosystem, include: Advantest, Alchip Technologies, Altos Design Automation, Cadence Design Systems, CEA/Leti, D2S, Dai Nippon Printing, e-Shuttle, eSilicon Corporation, Fastrack Design, Fujitsu Microelectronics, Magma Design Automation, Tela Innovations, Toppan Printing, Virage Logic and Vistec Electron Beam Lithography Group. The initiative also includes representatives from the design community who will serve in an advisory capacity, including: Marty Deneroff, director of engineering at D. E. Shaw Research; Jack Harding, chairman, president and CEO of eSilicon; Colin Harris, chief operating officer (COO) of PMC-Sierra; Riko Radojcic, principal engineer and manager at Qualcomm; and Jean-Pierre Geronimi, director of computer-aided design (CAD) at STMicroelectronics. The formal steering group for the eBeam Initiative consists of Advantest, CEA/Leti, D2S, e-Shuttle, Fujitsu Microelectronics and Vistec, with D2S serving as the managing sponsor.

Pressing Industry Need for the eBeam Initiative

The rising cost trends of advanced ICs show no signs of slowing down unless an entirely new manufacturing approach is adopted. With mask budgets doubling at every node, the application range and market for low-volume application-specific integrated circuits (ASICs) continue to shrink—challenging the future profitability of many applications. Without the need to rely on a lithography shift, DFEB maximizes and enhances current e-beam technology. By efficiently employing the e-beam direct-write (EbDW) approach, DFEB eliminates the cost of masks and can speed time-to-market by shortening the design-to-lithography process flow.

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In addition to the obvious advantages this will deliver to systems companies seeking early prototypes for testing, this type of DFEB approach can also dramatically impact a host of specific application fields, including low- to mid-volume semiconductor companies producing test chips, engineering samples and design derivatives.

With members representing the entire value chain, from intellectual property (IP) and electronic design automation (EDA) companies to semiconductor manufacturers and equipment makers, system design companies and research entities, service companies and mask makers, the initiative is expected to greatly accelerate production-oriented EbDW technology using DFEB.

“Through successful collaboration, we will be able to share and educate the industry on the myriad benefits afforded by this new maskless manufacturing approach,” stated Aki Fujimura, CEO of D2S. “Currently, the total available mask budget in the industry is extremely cost prohibitive. With DFEB, however, there will be a reduction in mask costs while enabling a larger variety of lower-volume SoCs.”

Colin Harris, COO of PMC-Sierra and an advisor for the eBeam Initiative, noted, “The growing interest we’re witnessing among many of today’s leaders demonstrates the strong potential DFEB holds to address the industry’s growing mask costs. By enabling a lower threshold to tapeout we will be able to adopt new technology nodes earlier and better target products for lower power and higher performance.”

Early Results Validate DFEB’s Success

Various eBeam Initiative members have already collaborated to validate maskless manufacturing with successful test wafers for the 45-nm and 32-nm nodes.

A related paper titled “Cell Projection Use in Maskless Lithography for 45-nm and 32-nm Logic Nodes” will be presented in Session 5: EBDW at 2:20 p.m., Tuesday, February 24, during SPIE’s Advanced Lithography Conference held in the San Jose McEnery Convention Center.

About Design for E-beam (DFEB)

DFEB is a design-to-manufacturing approach to enhance the throughput of e-beam (EB) lithographic exposure. DFEB uses character or cell projection (CP) technology combined with design and software techniques to reduce a design's required shot count, resulting in increased CP e-beam direct-write (EbDW) throughput. A new technology backgrounder on DFEB is available on the eBeam Initiative website, www.ebeam.org.

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About The eBeam Initiative

The eBeam Initiative provides a forum for educational and promotional activities regarding a new design-to-manufacturing approach, known as design for e-beam (DFEB). DFEB reduces mask costs for semiconductor devices by combining design, design software, manufacturing, manufacturing equipment and manufacturing software expertise. The goals of the Initiative are to reduce the barriers to adoption to enable more integrated circuit (IC) design starts and faster time-to-market while increasing the investment in DFEB throughout the semiconductor ecosystem.

Members, advisors and the steering group, which span the semiconductor ecosystem, include: Advantest, Alchip Technologies, Altos Design Automation, Cadence Design Systems, CEA/Leti, D2S, Dai Nippon Printing, D. E. Shaw Research, e-Shuttle, eSilicon Corporation, Fastrack Design, Fujitsu Microelectronics, Magma Design Automation, PMC-Sierra, Qualcomm, STMicroelectronics, Tela Innovations, Toppan Printing, Virage Logic and Vistec Electron Beam Lithography Group. Membership is open to all companies and institutions throughout the electronics industry. To find out more, please visit www.ebeam.org.

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