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EBEAM INITIATIVE INTRODUCES DESIGN FOR E-BEAM METHODOLOGY GUIDELINES AND TRAINING COURSES

Guidelines and Training Build on Milestones Achieved During 2009

SAN JOSE, Calif., November 9, 2009—The eBeam Initiative, a forum dedicated to the education and promotion of a new design-to-manufacturing approach known as design for e-beam (DFEB), today announced the availability of DFEB methodology guidelines and training sessions for physical design engineers, which will be made available to members and non-members. DFEB is a design-tomanufacturing approach to enhance the throughput of e-beam (EB) lithographic exposure. During 2009, eBeam Initiative members collaborated on manufacturability proof points, silicon validation of the DFEB design methodology and validation of the Packed Stencil technology to further enhance EB throughput. The guidelines and training reflect the tangible progress on the Initiative's roadmap and its mission to educate the semiconductor community about DFEB.

The first version of the DFEB methodology guidelines will be made available on November 9, 2009 and can be accessed by going to www.ebeam.org. On November 24, 2009 Cadence Design Systems Japan will host a morning and afternoon DFEB training session at its Shin-Yokohama office with the training conducted in Japanese. The local training is scheduled for December 9, 2009 in building 8 of Cadence Design Systems' San Jose, Calif. office. Cadence Design Systems, D2S and e-Shuttle are sponsoring the training sessions at no cost to attendees. For both locations, the morning session will take place from 10:00 a.m.-1:00 p.m. (includes lunch) and is intended for management and physical design engineers. The afternoon segment is dedicated to physical design engineers only and will run from 1:00 p.m.—3:00 p.m. Registration is now open via the Initiative's website.

"These educational tools will demonstrate the DFEB benefits to the design community as well as educate them about the technology trends in e-beam manufacturing," stated Aki Fujimura, CEO of D2S and managing sponsor of the eBeam Initiative. "Providing methodology guidelines and training sessions at this time reflects great progress by the Initiative members in validating the DFEB methodology in 2009 consistent with the Initiative's roadmap."

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EBEAM INTRODUCES DEEB METHODOLOGY GUIDELINES AND TRAINING COURSES.......PAGE 2 OF 2

The eBeam Initiative was launched in February 2009 and includes a total of 21 leading companies throughout the entire semiconductor ecosystem to promote DFEB technology. Further details of the eBeam Initiative can be found at www.ebeam.org.

U.S. Training Course

Cadence Design Systems 2655 Seely Avenue San Jose, CA 95134

Japan Training Course

Cadence Design Systems Japan 2-100-45 Shin-Yokohama, Kohoku-ku Yokohama 222-0033, Japan

About Design for E-beam (DFEB)

DFEB is a design-to-manufacturing approach to enhance the throughput of e-beam (EB) lithographic exposure. DFEB uses character or cell projection (CP) technology combined with design and software techniques to reduce a design's required shot count, resulting in increased CP e-beam direct-write (EbDW) throughput. A new technology backgrounder on DFEB is available on the eBeam Initiative website, www.ebeam.org.

About The eBeam Initiative

The eBeam Initiative provides a forum for educational and promotional activities regarding a new design-to-manufacturing approach, known as design for e-beam (DFEB). DFEB reduces mask costs for semiconductor devices by combining design, design software, manufacturing, manufacturing equipment and manufacturing software expertise. The goals of the Initiative are to reduce the barriers to adoption to enable more integrated circuit (IC) design starts and faster time-to-market while increasing the investment in DFEB throughout the semiconductor ecosystem. Members and advisors, which span the semiconductor ecosystem, include: Advantest, Alchip Technologies, Altos Design Automation, Cadence Design Systems, CEA/Leti, D2S, Dai Nippon Printing, Marty Deneroff from D. E. Shaw Research, e-Shuttle, Jack Harding from eSilicon Corporation, Fastrack Design, Fujitsu Microelectronics, GenISys GmbH, Magma Design Automation, Colin Harris from PMC-Sierra, Riko Radojcic from Qualcomm, STMicroelectronics, Tela Innovations, Toppan Printing, Virage Logic and Vistec Electron Beam Lithography Group. Membership is open to all companies and institutions throughout the electronics industry. To find out more, please visit www.ebeam.org.

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