Integrated Mask/Lithography Signoff Verification using a Virtual VSB Writer

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What happens when mask hotspots escape the mask shop?

Mask hotspots are real today

MEEF Assumptions Are Overly Optimistic

ITRS Roadmap

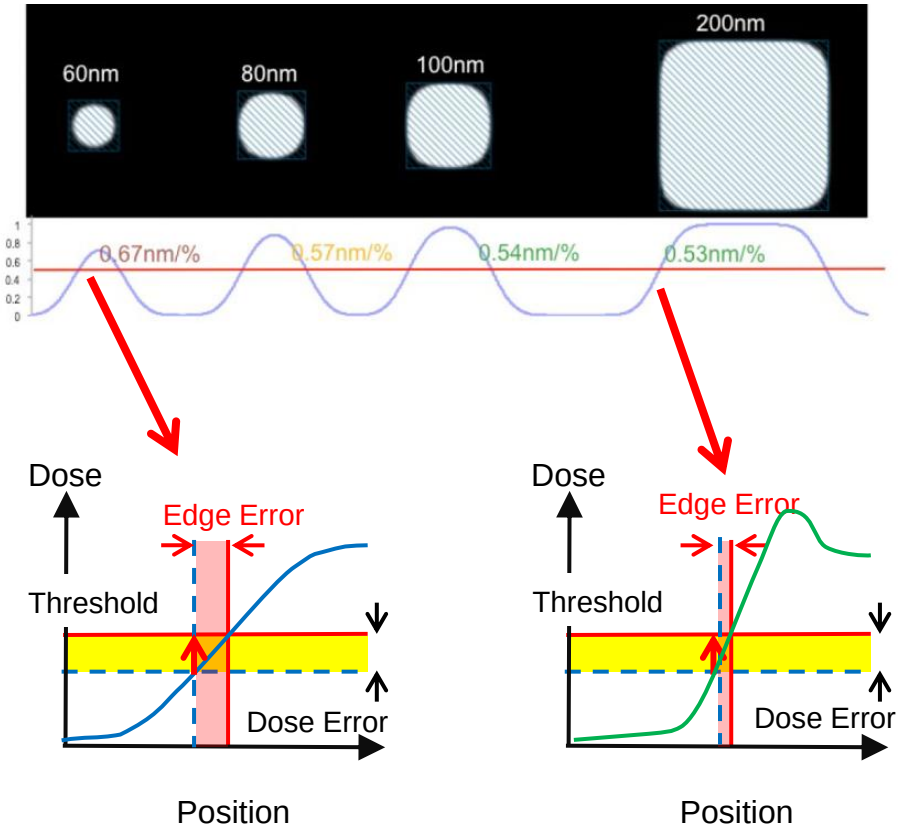
- Mask CDU Requirements: ↓ (0.5-0.9nm)
- MEEF: ↑ (4-8)

Why things are not OK!

- MEEF typically assumes a globally uniform isotropic variability error.
- This is optimistic.
  - Small mask features have poorer mask process margins and inherently higher variability than standard mask process control structures.
  - **Effectively**, MEEF may be larger for some of these critical structures.

Sources of Mask Errors:
CD Non-uniformity due to Mask Process Variation

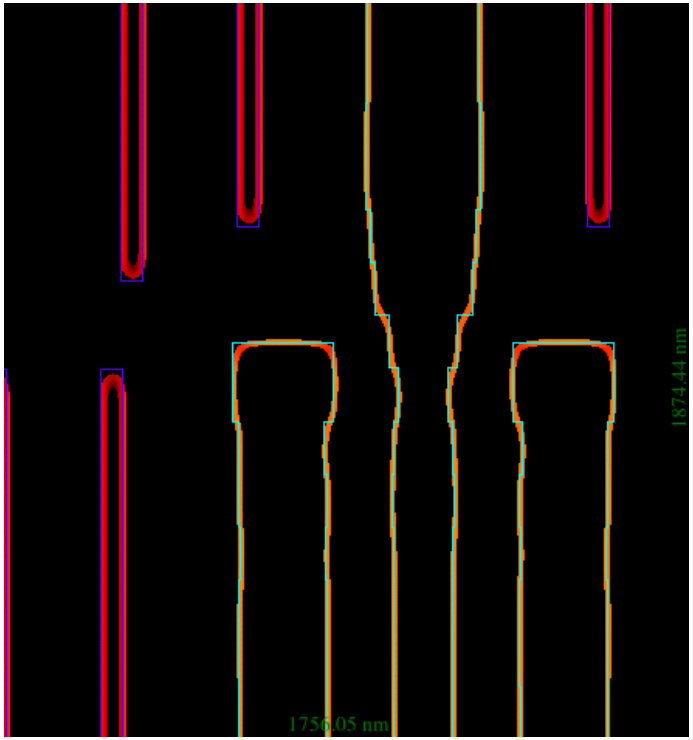
Simulate mask pattern exposures on the mask with resulting edge profiles below.



I've never met a mask error that couldn't be modeled by dose variation.

Process variation causes larger edge position errors for smaller shapes.

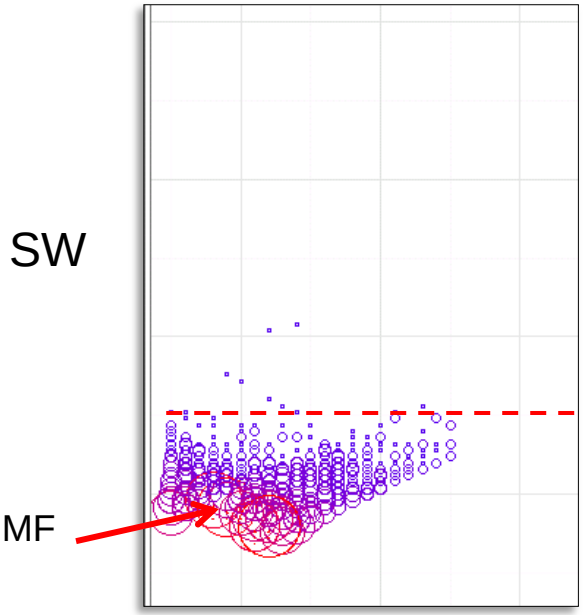
Which Mask Errors Matter?



- Red >= 1nm / %Dose error (4X)

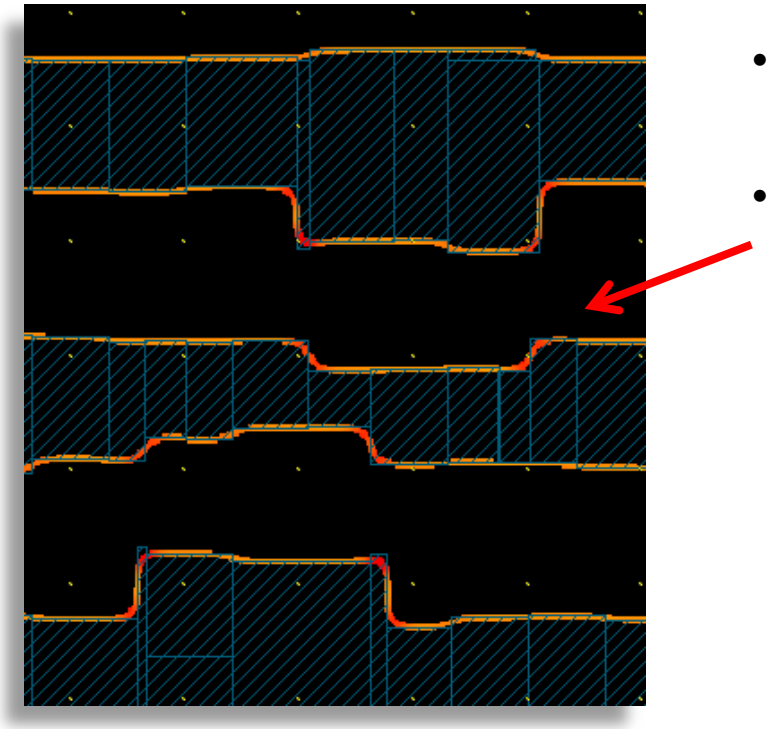
- Just because a mask pattern has poor dose margin it does not mean that it will impact the wafer.
- For example, in most contexts, the Main Feature is very robust to SRAF errors
- A variation analysis can confirm the criticality of a feature.

Main Feature CD Error due to SRAF error



Critical Regions of High Variability

- OPC Mask designs may include features that are intrinsically highly-variable

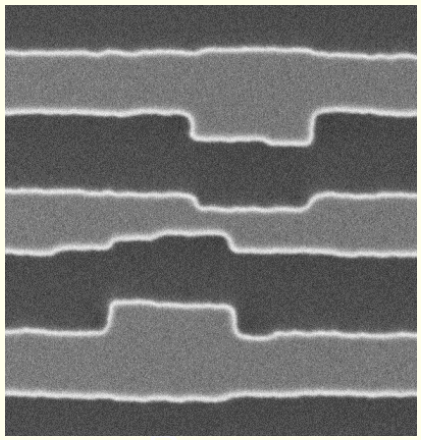


- Poor Dose Margin Error regions flagged in Red (1nm/%-dose (4X))
- The number of Poor Dose Margin corners may significantly impact the CD as well.

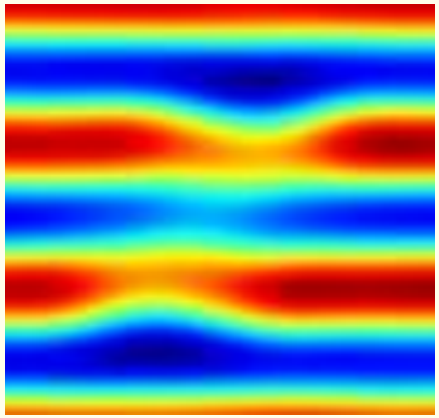
Dual Mask/Wafer Simulation Now Correlates to Silicon

Real Mask

SEM

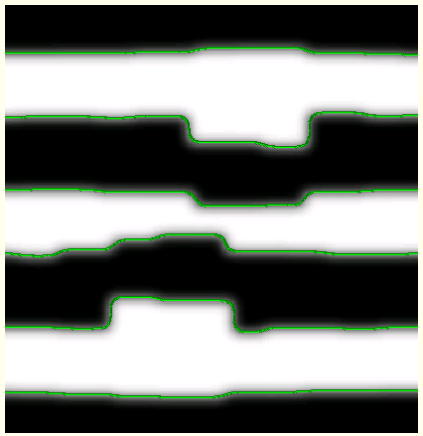


AIMS



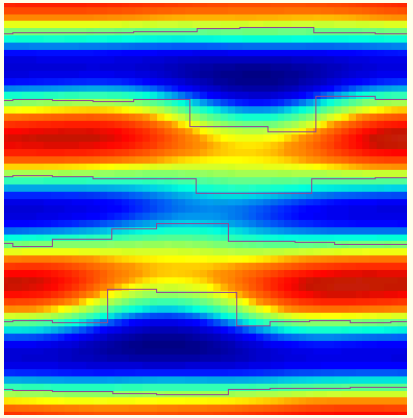
Simulated Mask

- Simulate the impact of mask VSB write and process



Simulated Mask + Litho

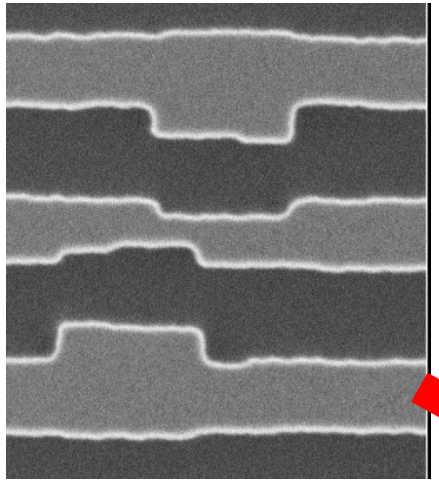
- Simulate the wafer aerial image from the simulated mask image.



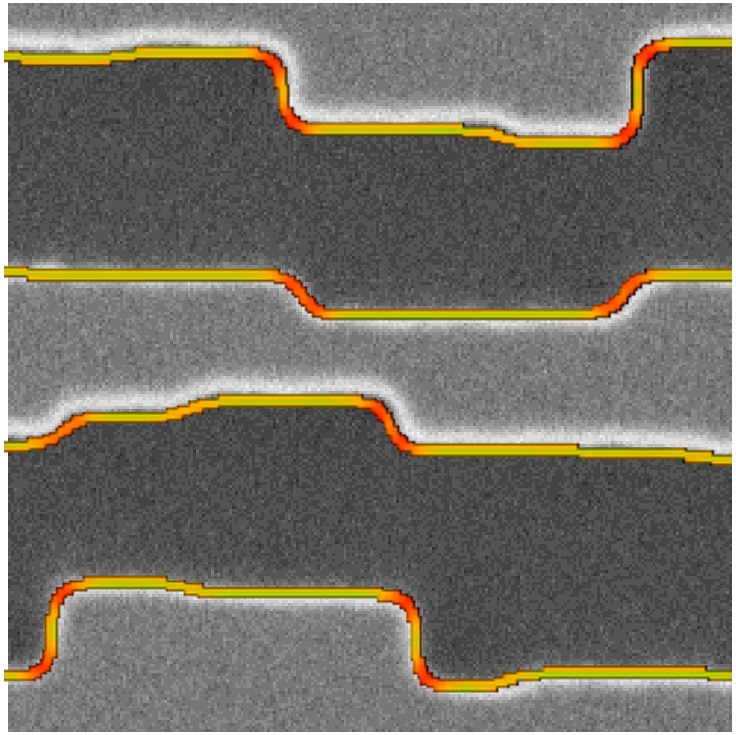
D2S TrueMask® DS

Simulation Accuracy of Mask Shape and Variability

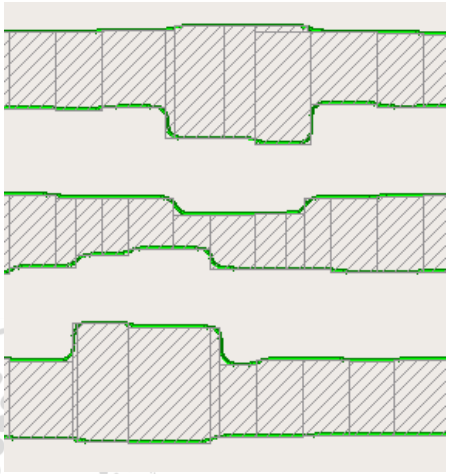
Mask SEM



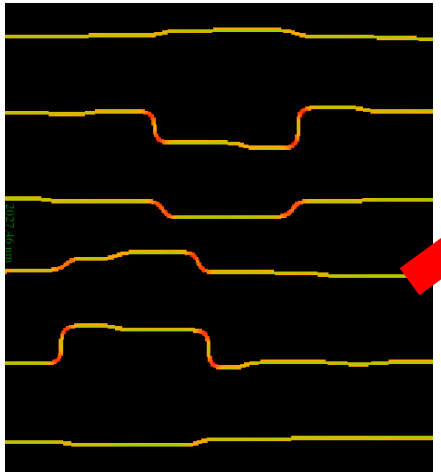
Simulation is able to very accurately simulate the mask shape for VSB e-beam litho



Simulated mask contours



Simulated high variability mask regions

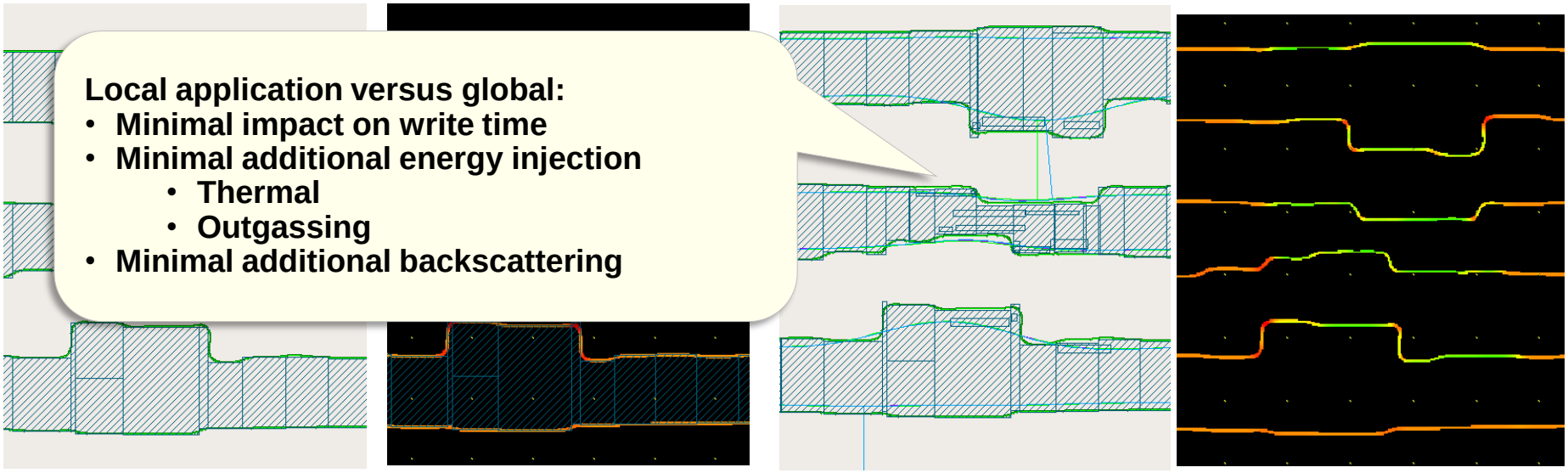


What to do if a High-MEEF/Poor Dose Margin Region is Found

- Poor Dose Margin regions may be improved by selective dose assignment and/or model-based overlapping shot methods such as MB-MDP to reduce the local Mask CD variation.

MEEF = 4.7

Equivalent-MEEF = 3.0



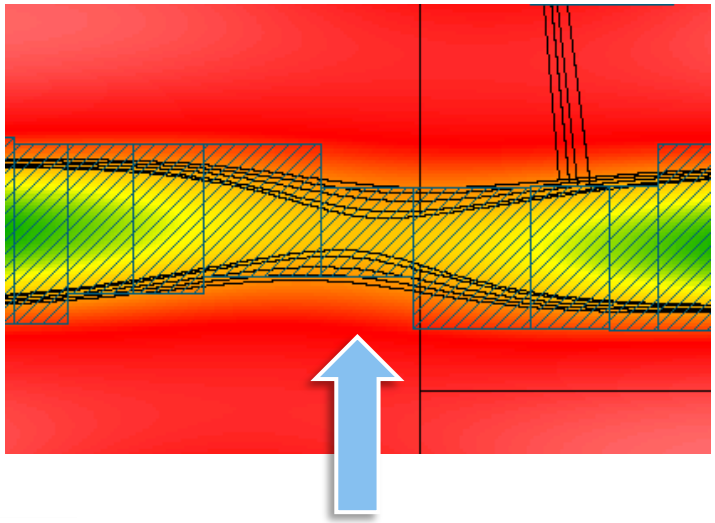
Red: Dose Margin Error = 1nm/%dose error

Green: Dose Margin Error = 0.5nm/%dose error

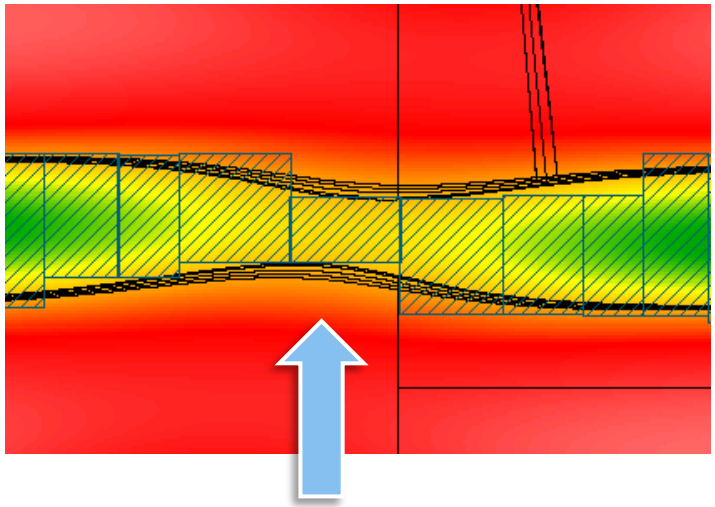
Impact of Process Variation
Litho Aerial Image Contours at Different VSB Doses

- Integrated VSB Mask Simulation and Litho Simulation illustrates impact of local mask dose margin on litho sensitivity.
- The OPC same region with enhanced dose margin is far more resilient to VSB mask writer and other mask manufacturing variations.

Conventional Mask
Poor Dose Margin



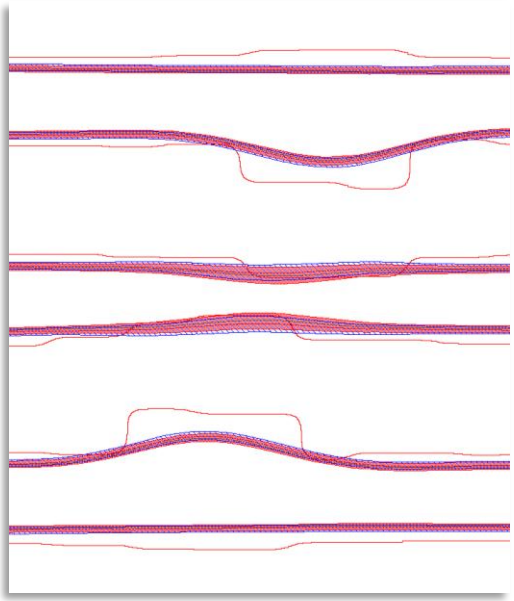
Dose Enhanced Mask

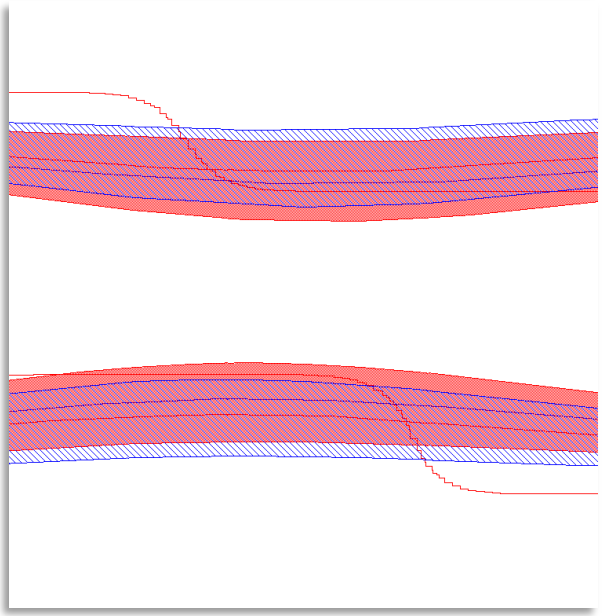


Dual Mask/Wafer lithography pinching at various degrees of mask manufacturing error…
Traditional MEEF will underestimate this.

Integrate the Simulated Masks with Production OPC

- Highly-calibrated production litho/dev/etch model
- Litho PV Band: E+/- , Def+/-
- Mask PV Band: Read in simulated masks (TrueMask DS) over Dose-Ranges and do ORC simulations/verification from that
- Nominal and PV Band significantly improved for MB-MDP Enhanced Mask.



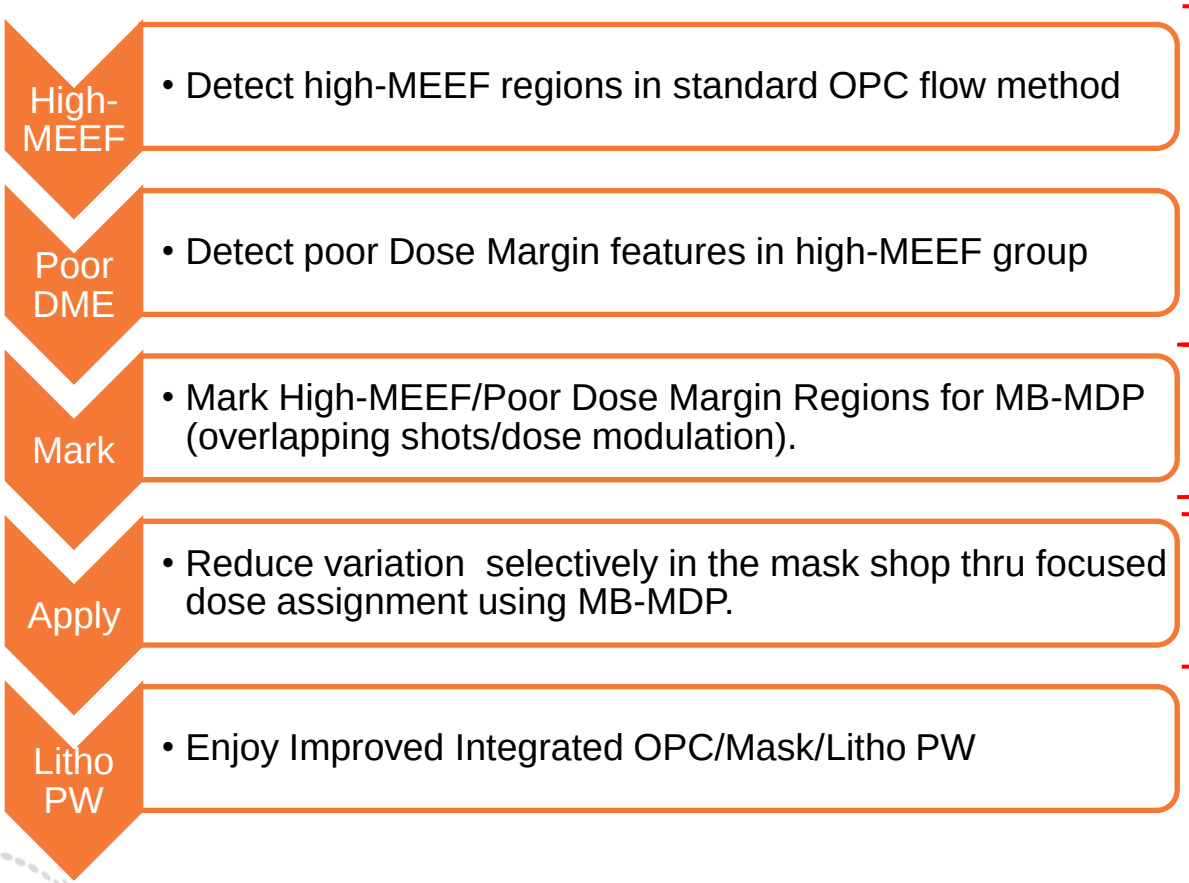


Conventional (Inside)
Enhanced DM (Outside)

- We can also read in SEM image contours and do ORC simulations/verification from those to augment reality.

One Integrated Flow that's Possible Today

Judiciously select features in an OPC mask design which may be improved by Dose Margin enhancement.



Where is there a high likelihood for mask-induced failure?

Feed forward cooperation.

Very specific mask enhancements to minimize shot count/back scattering/thermal increase.

Summary – Catching Mask Hotspots

- Mask process variations can create errors undetectable in the mask shop which impact silicon functionality.
- These variations may not be modeled with sufficient accuracy in OPC flows.

We propose a systematic integrated verification method that comprehends mask AND litho variations and minimizes the potential for long-loop iterations with mask and silicon … *before* OPC tapeout.

Thank you!

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