

The Need for Speed: Computations for EUV Lithography

EUV lithography implemented at different node than originally conceived

Summary

EUVL is the only viable solution for 45 nm

- Integration of all EUVL modules demonstrated feasibility of the EUVL technology
- Mask costs are affordable – defect mitigation and repair methods demonstrated
- Suppliers are engaged to commercialize the technology
- Remaining technical challenges have been identified and are actively being addressed
- Commercialization emphasis is required

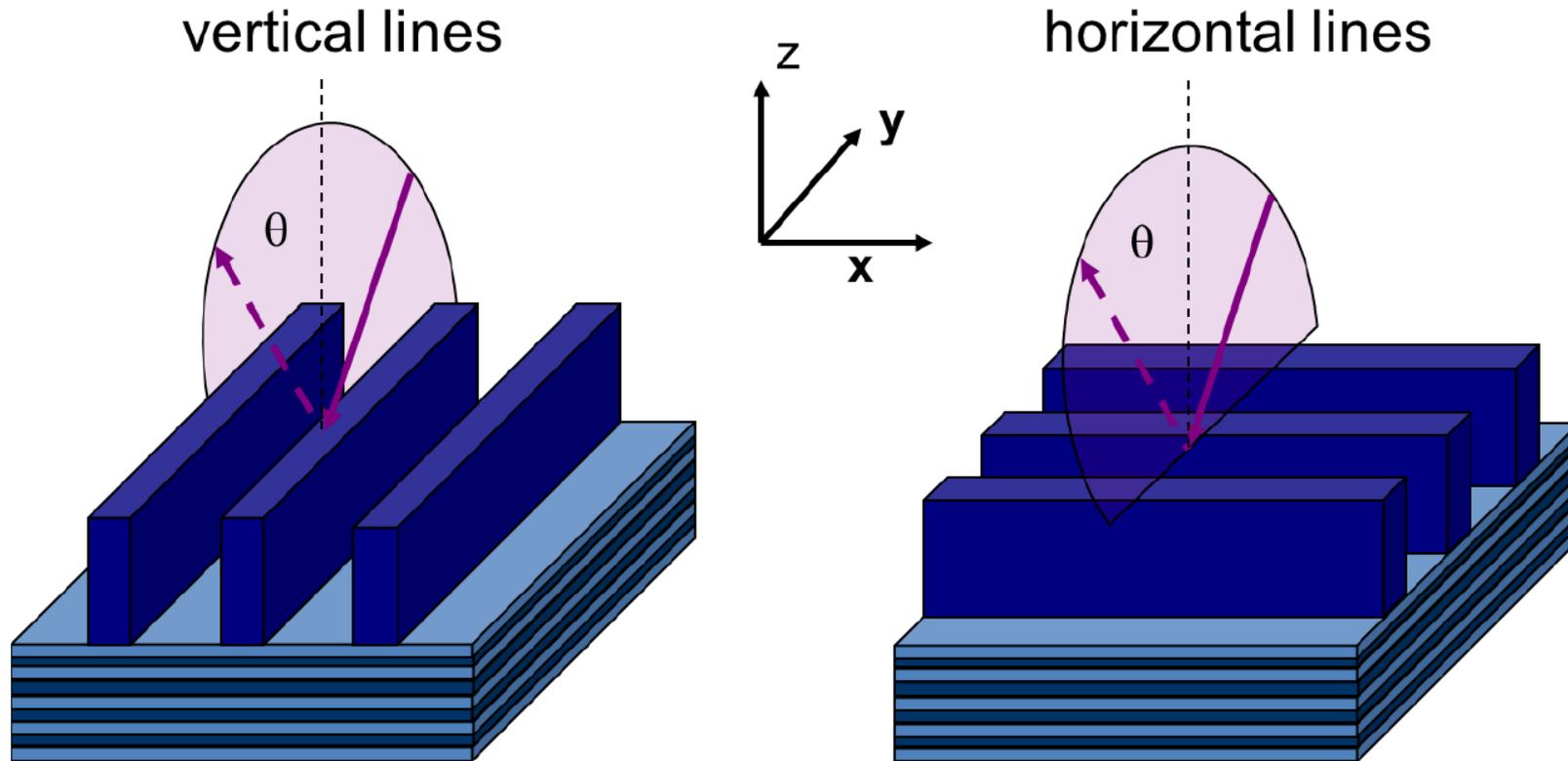
Gwyn:PMJ:4/17/03:27



Gwyn and Silverman,
“EUV Lithography
Transition from Research
to Commercialization,”
Photomask Japan, 2003

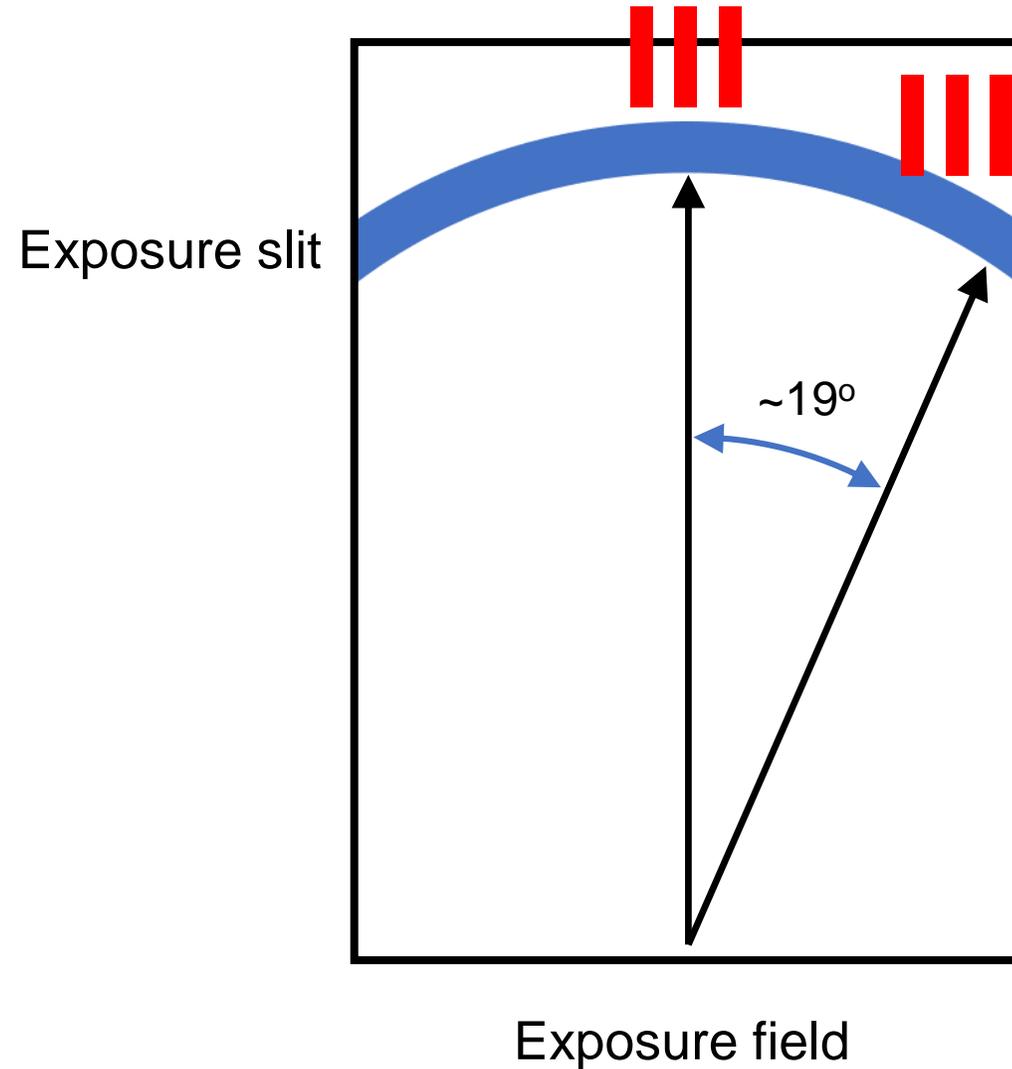
Minimum pitch = 160 nm

Horizontal-vertical bias due to oblique illumination



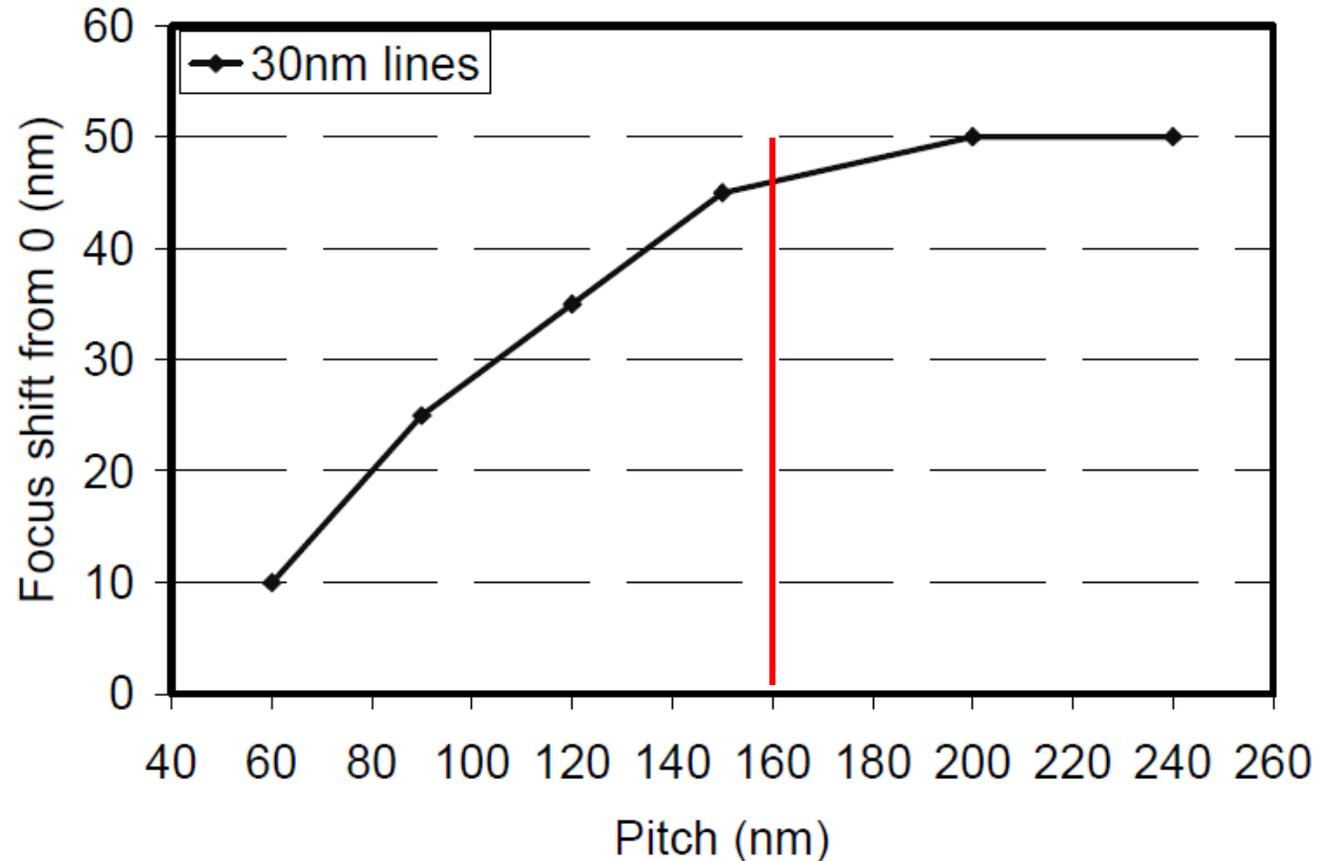
Erdmann, et al.
"Characterization and mitigation of 3D mask effects in extreme ultraviolet lithography."
Advanced Optical Technologies 6, no. 3-4 (2017)

Biases in-between



- Ring-field optics have long been used in scanning lithography
 - Reduced aberrations

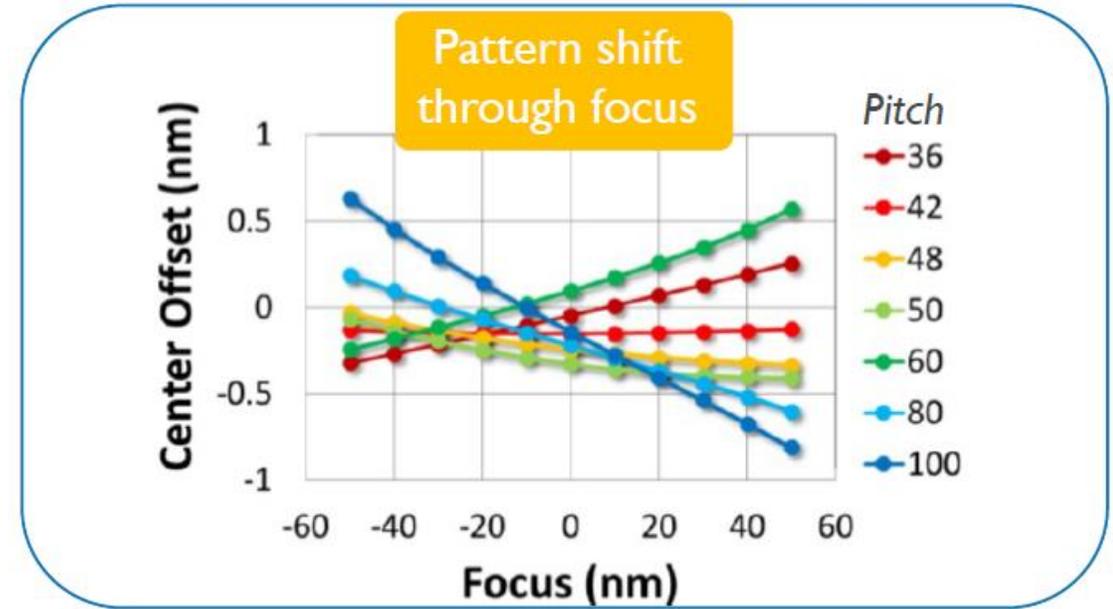
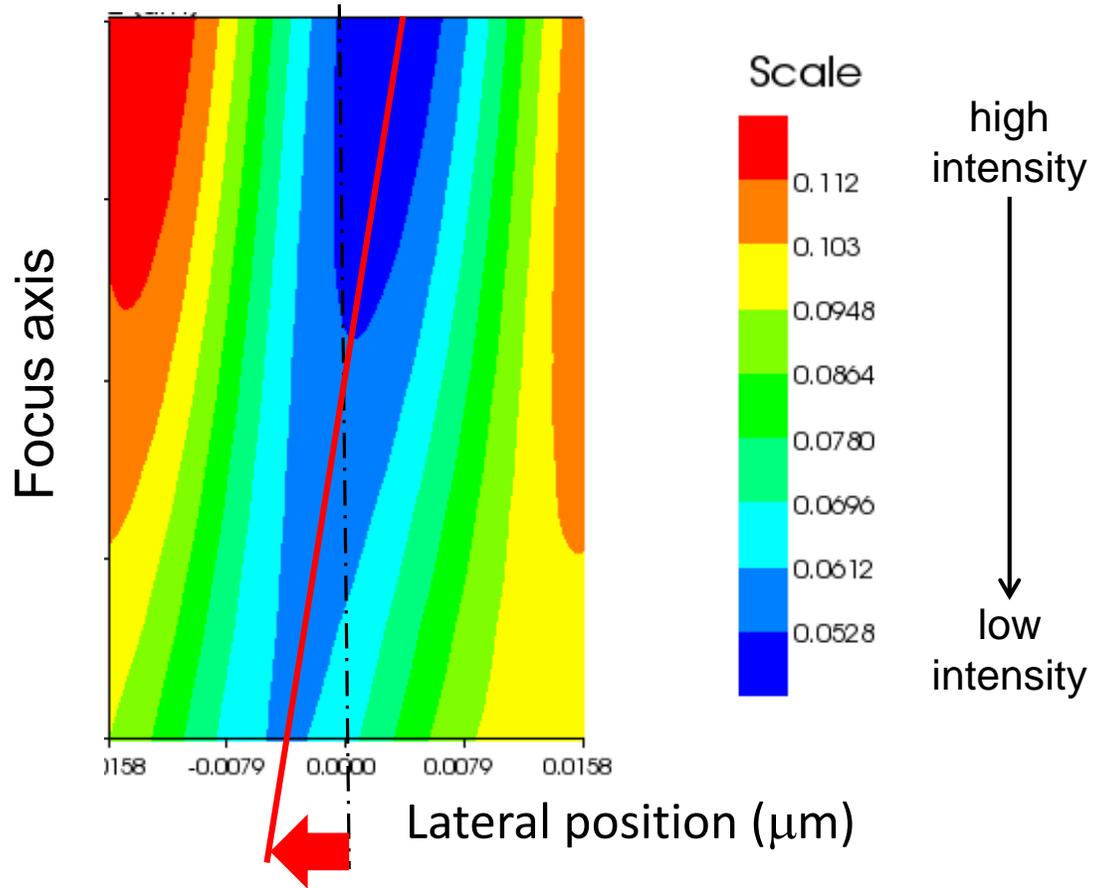
Mask 3D effects were recognized early: Pitch dependence for focus



Pei-Yang Yan,
“Understanding Bossung Curve
Asymmetry and Focus Shift
Effect in EUV Lithography,”
BACUS Symposium on
Photomask Technology,
2001

Fig. 2. Focus shift as a function of pitch for 30nm lines.
The light incident angle is 5-degree.

Pattern placement errors through focus



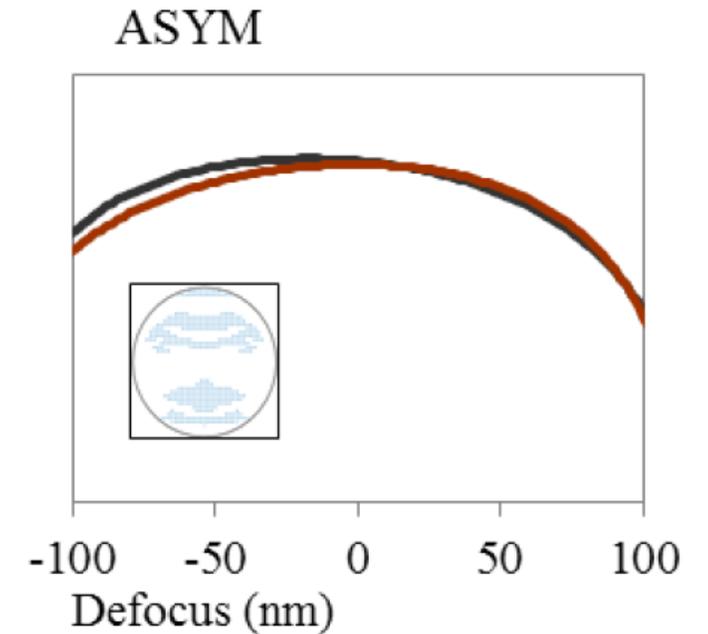
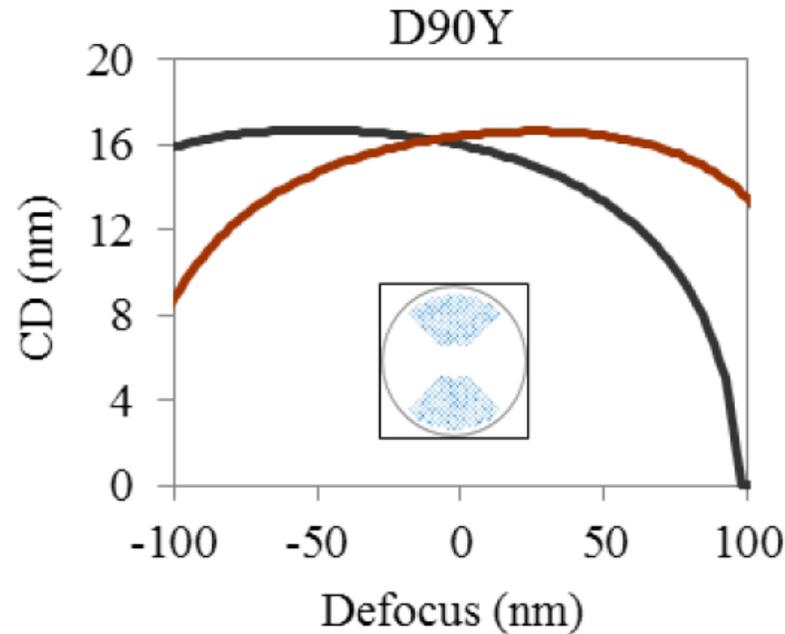
L. Van Look, et al.,
 “Mask 3D Effect Mitigation by Source
 Optimization and Assist Feature Placement”
 (2016)

S. Raghunathan, et al., “Characterization of
 Telecentricity Errors in High-Numerical-Aperture
 Extreme Ultraviolet Mask Images,” 3-beams (2014)

**This is new: Overlay needs to be considered
 when employing process window-aware OPC!**

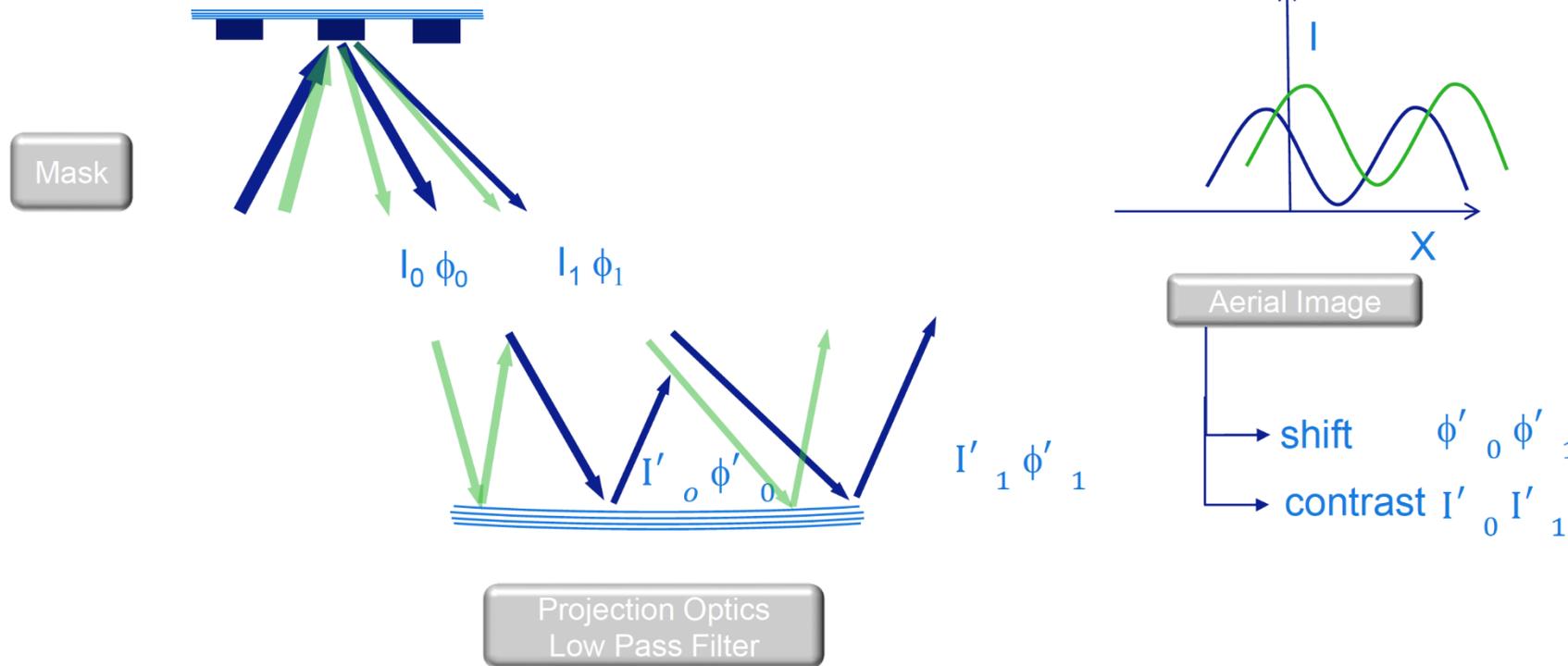
Mask 3D effects drive need for complex illumination

CD versus focus for 2-bar structures, 32 nm pitch:



T. Last, et al. "Illumination pupil optimization in 0.33-NA extreme ultraviolet lithography by intensity balancing for semi-isolated dark field two-bar M1 building blocks," JM3 (2016)

Image blurring due to mask 3D effects



Images from different source points are displaced laterally

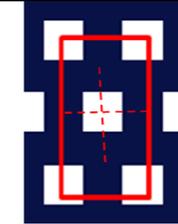
→ extended sources result in blurred images

Jo Finders, 2017 EUVL Symposium

21 nm hp image blurring example

2 Looking at aerial image shift @BF

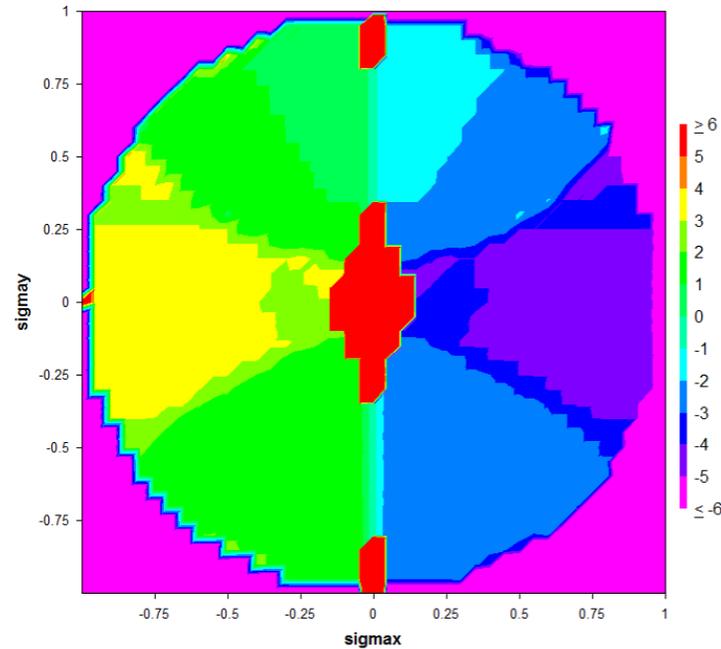
Shifts up to $\pm 5\text{nm}$



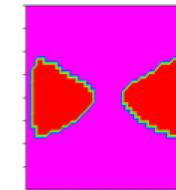
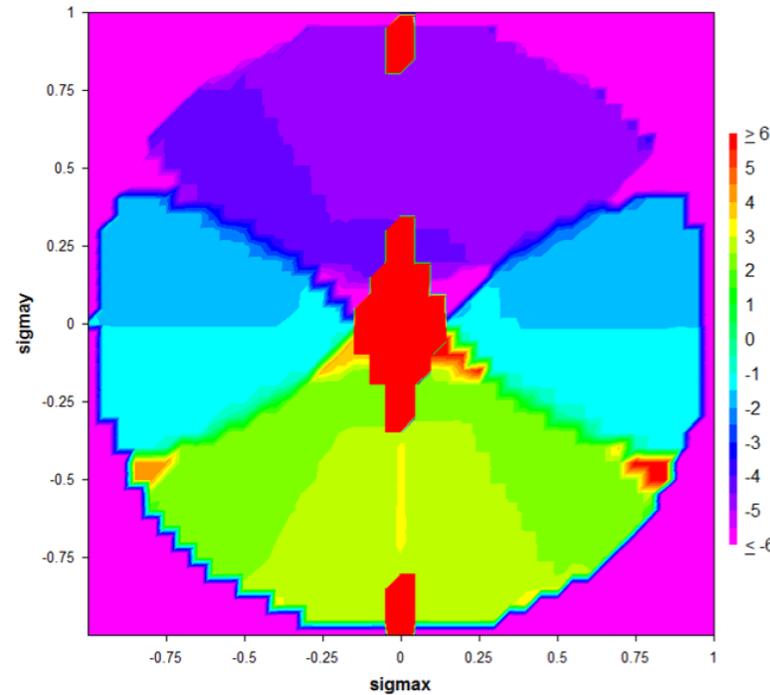
ASML

Public
Slide 14
<Date>

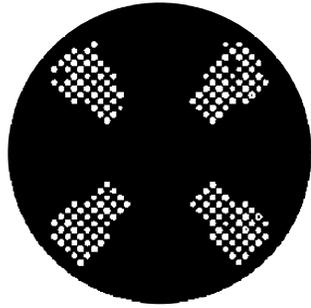
Cutline x



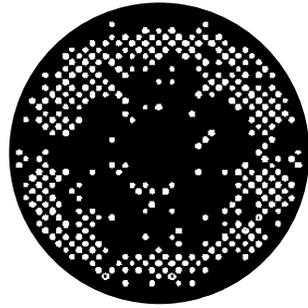
Cutline y



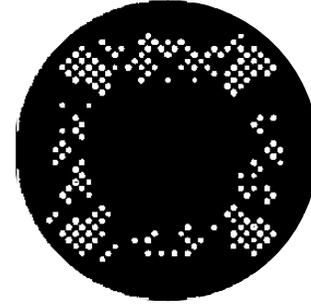
Need to maintain normalized image log-slope (NILS) to address LER



Quadrupole illumination

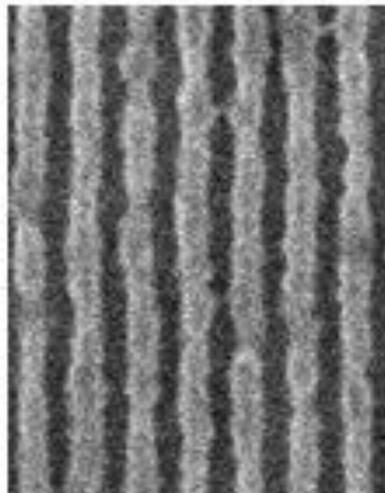


SMO standard solution

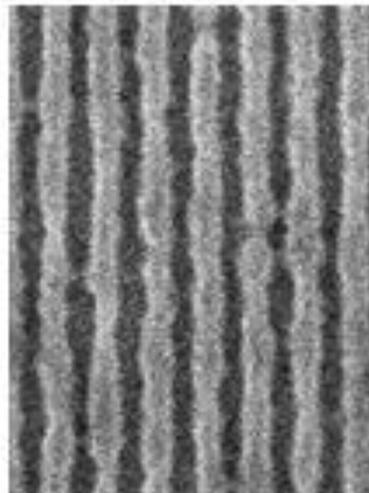


SMO Nils optimized

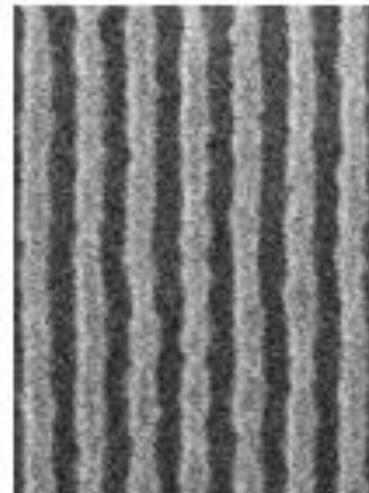
32-nm pitch lines/spaces



NILS = 1.61
LER = 3.6 nm



NILS = 1.57
LER = 3.7 nm



NILS = 2.05
LER = 2.6 nm

"Application of EUV resolution enhancement techniques (RET) to optimize and extend single exposure bi-directional patterning for 7nm and beyond logic designs"

Ryoung-Han Kim et. al.,
SPIE Advanced Lithography Symposium (2016)

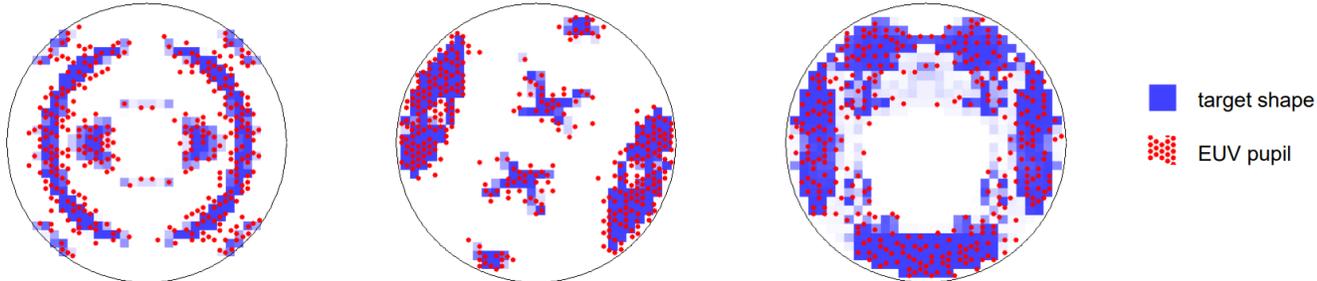
Freeform illumination is now available for EUV lithography

Freeform pupil shapes 

SMO pupil
for logic cut mask

rotated pupil shape
for DRAM brickwalls

y-asymmetric
3D mask compensation



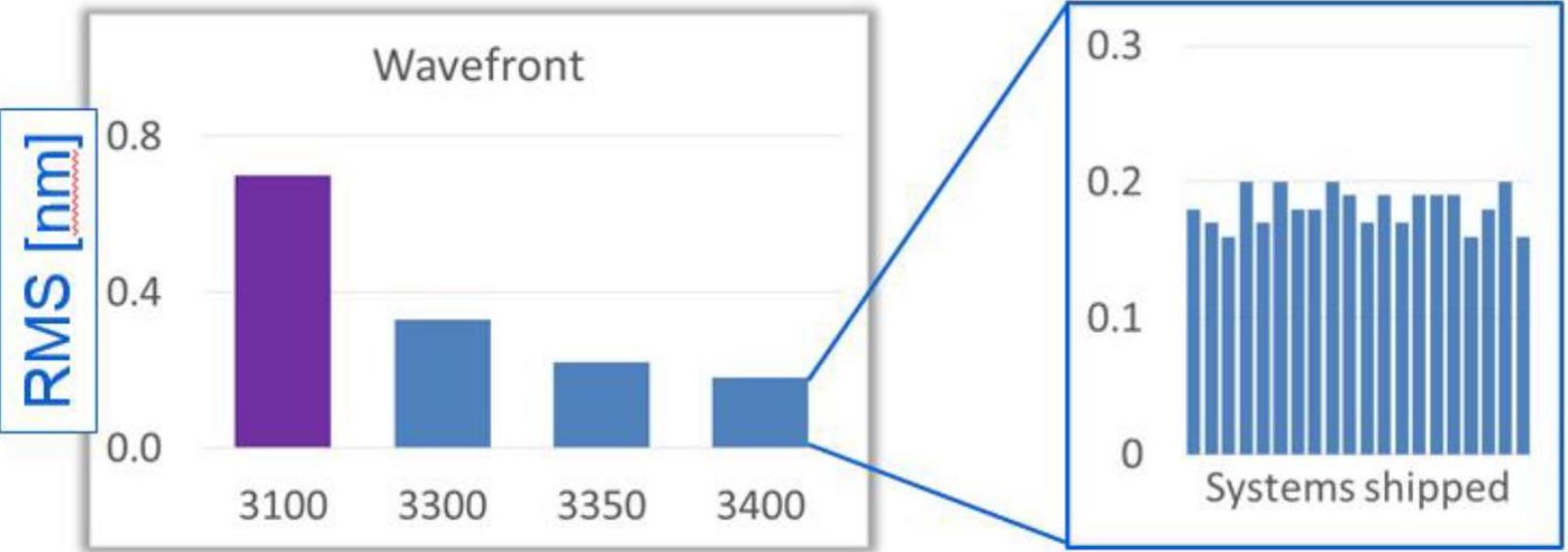
■ target shape
■ EUV pupil

all examples without light loss (100% illuminator efficiency) on Starlith® 3400 illumination system

Carl Zeiss SMT, Jack Liddle (Zeiss), Joerg Zimmermann (Zeiss), Jens Timo Neumann (Zeiss), Matthias Roesch (Zeiss), Ralf Gehrke (Zeiss), Bernhard Kneer (Zeiss), Felco van Setten (ASML), Jan van Schoot (ASML), Mark van de Kerkhof (ASML)

2017-06-15 10

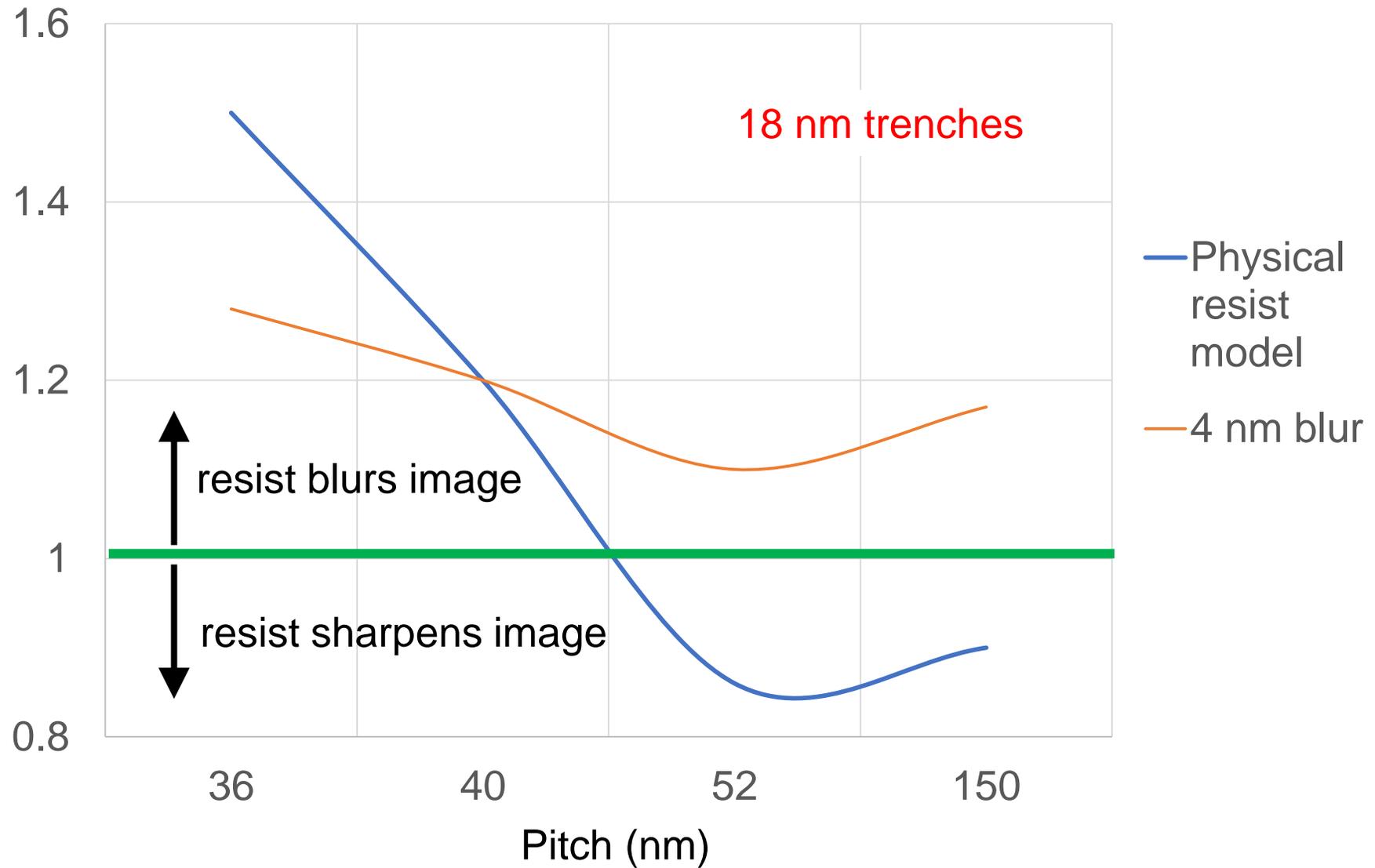
Aberrations are significant for EUV lithography



0.2 nm = 15 mλ

Winfried Kaiser, Semicon Korea, 2018

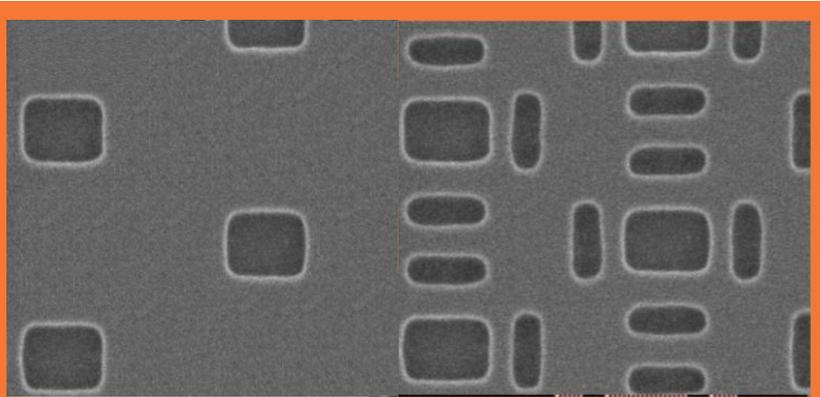
Complex resist physics



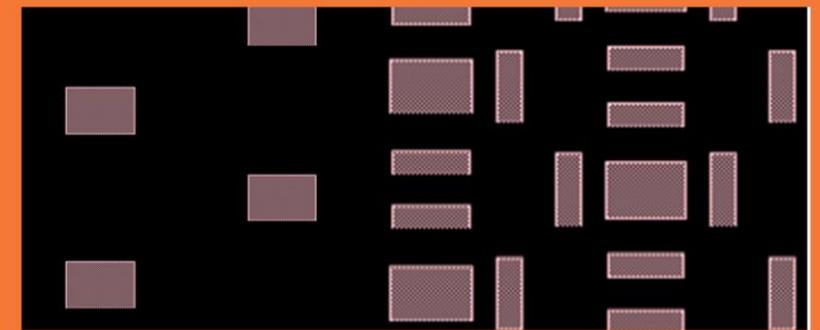
- OPC models need to contend with pitch-dependent resist-blur

Adapted from S. Hansen, JM3

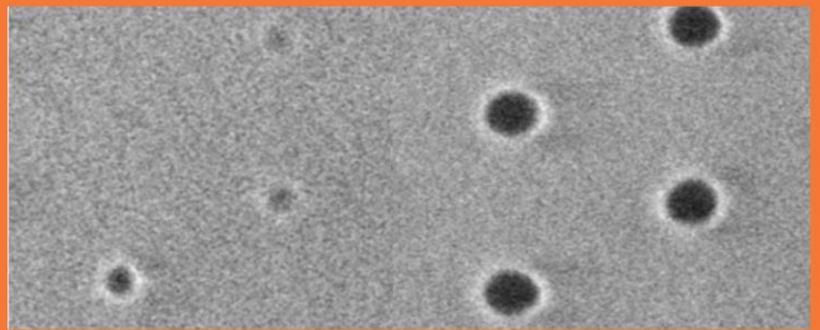
Sub-resolution assist features (SRAFs) for EUV lithography



Mask SEM
image



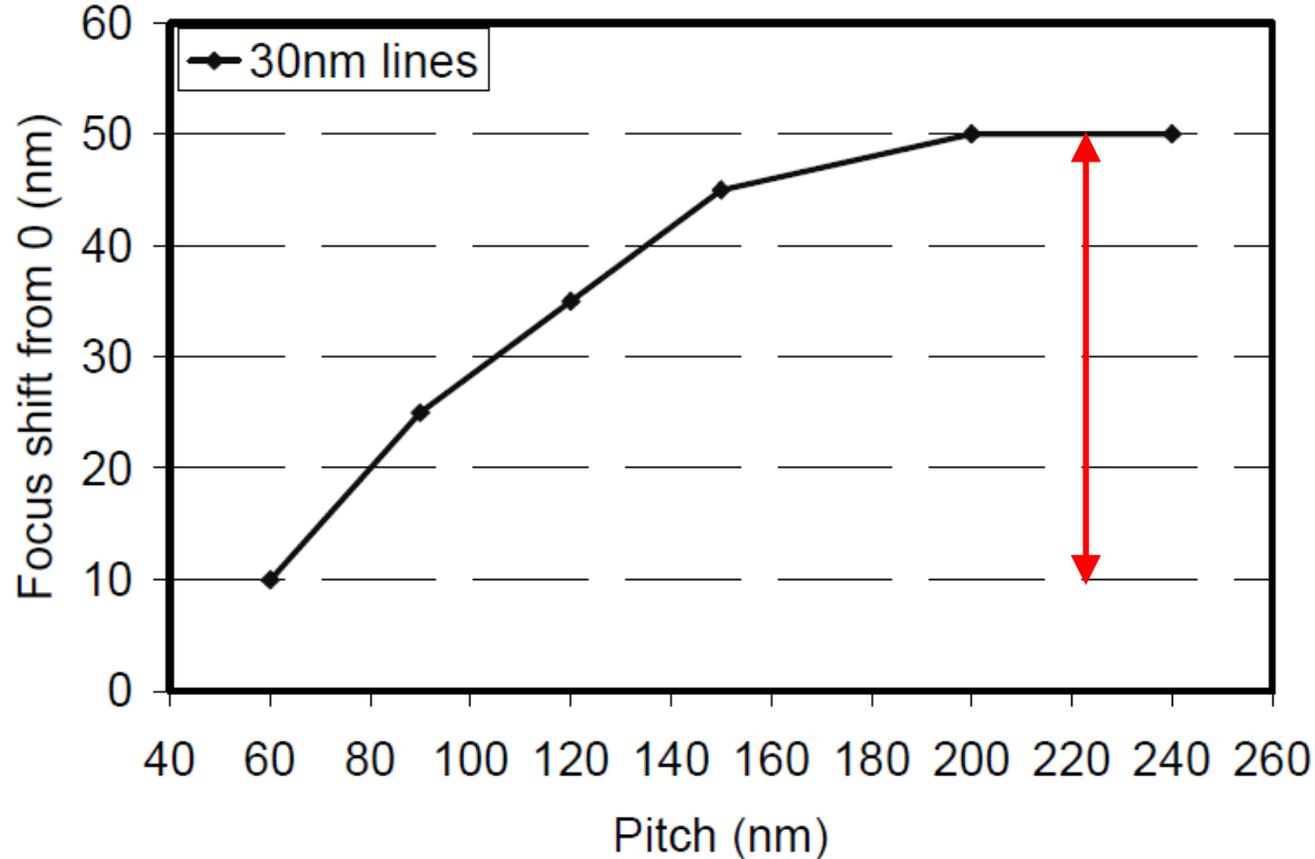
Design
layout



Developed resist
on-wafer SEM image

Deniz Civay, et al.,
“Subresolution assist features in
extreme ultraviolet lithography,”
JM3 (2015)

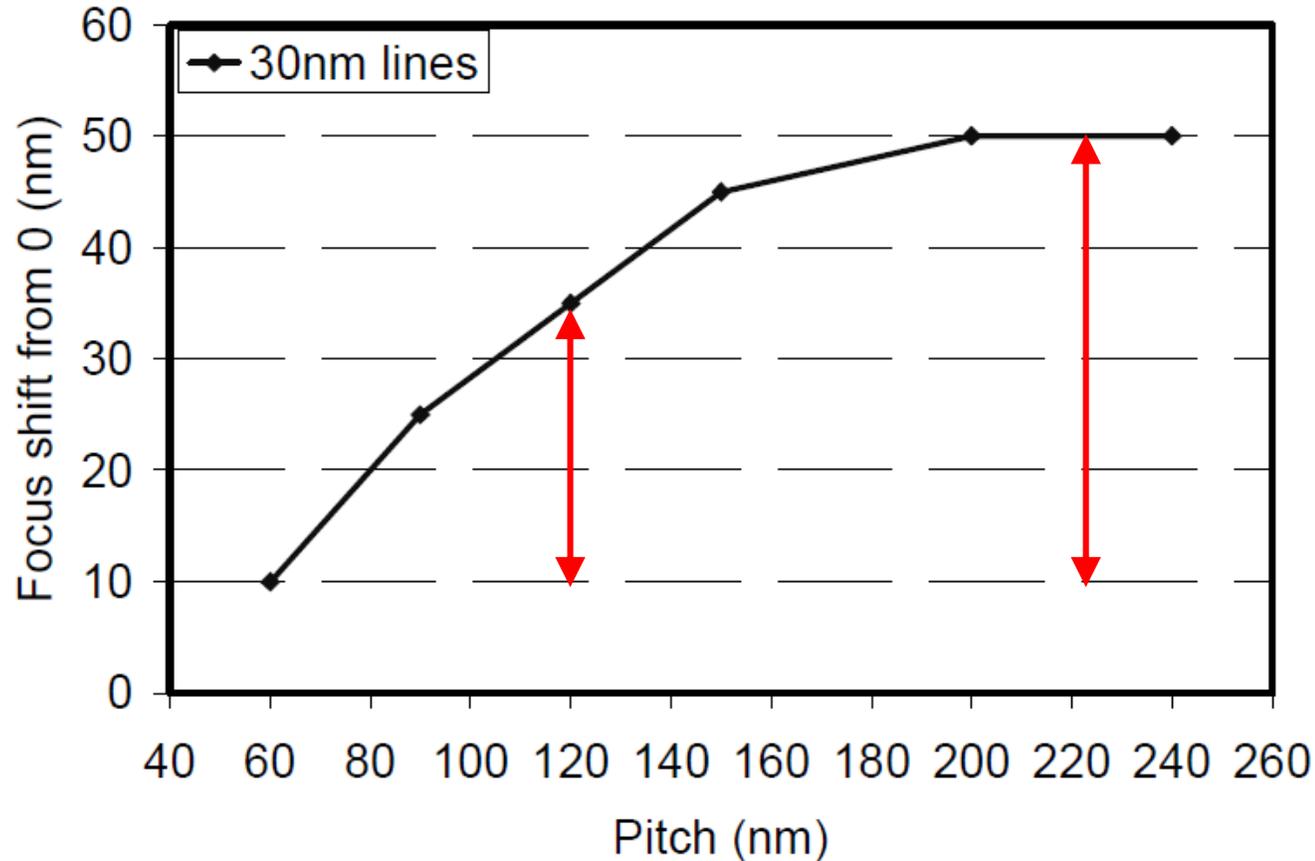
Application of SRAFs significantly reduces range of focus shifts



Pei-Yang Yan,
“Understanding Bossung Curve
Asymmetry and Focus Shift
Effect in EUV Lithography,”
BACUS Symposium on
Photomask Technology,
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Fig. 2. Focus shift as a function of pitch for 30nm lines.
The light incident angle is 5-degree.

Application of SRAFs significantly reduces range of focus shifts



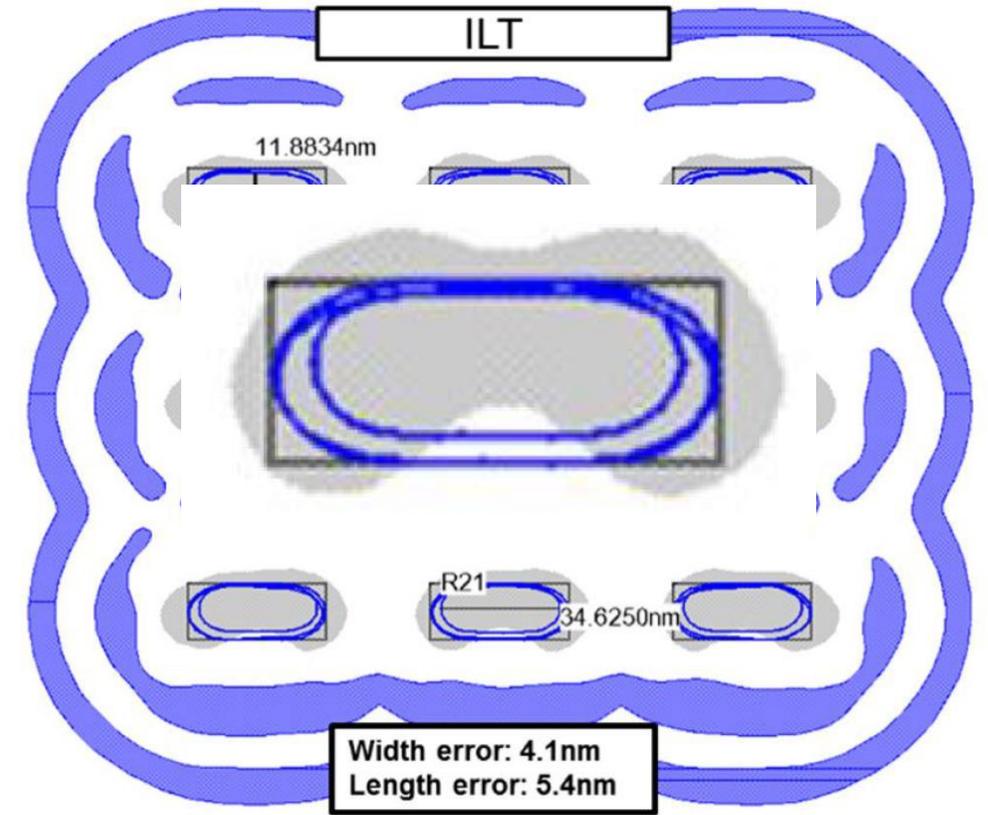
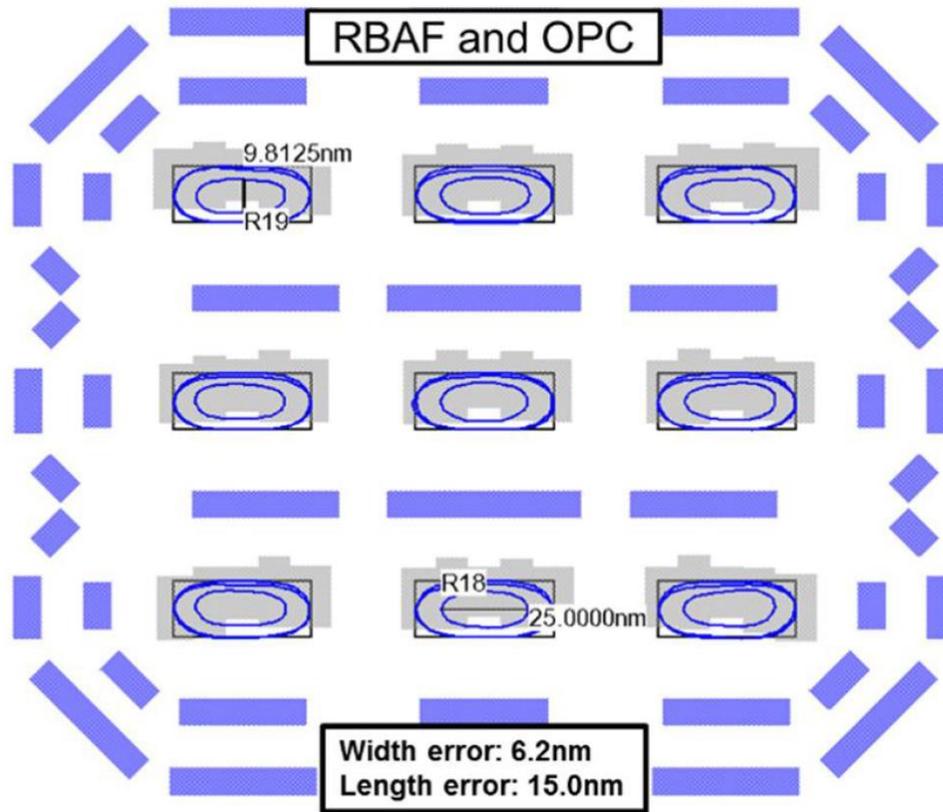
~40% reduction in
best focus variation

Pei-Yang Yan,
“Understanding Bossung Curve
Asymmetry and Focus Shift
Effect in EUV Lithography,”
BACUS Symposium on
Photomask Technology,
2001

Fig. 2. Focus shift as a function of pitch for 30nm lines.
The light incident angle is 5-degree.

The future is curvilinear

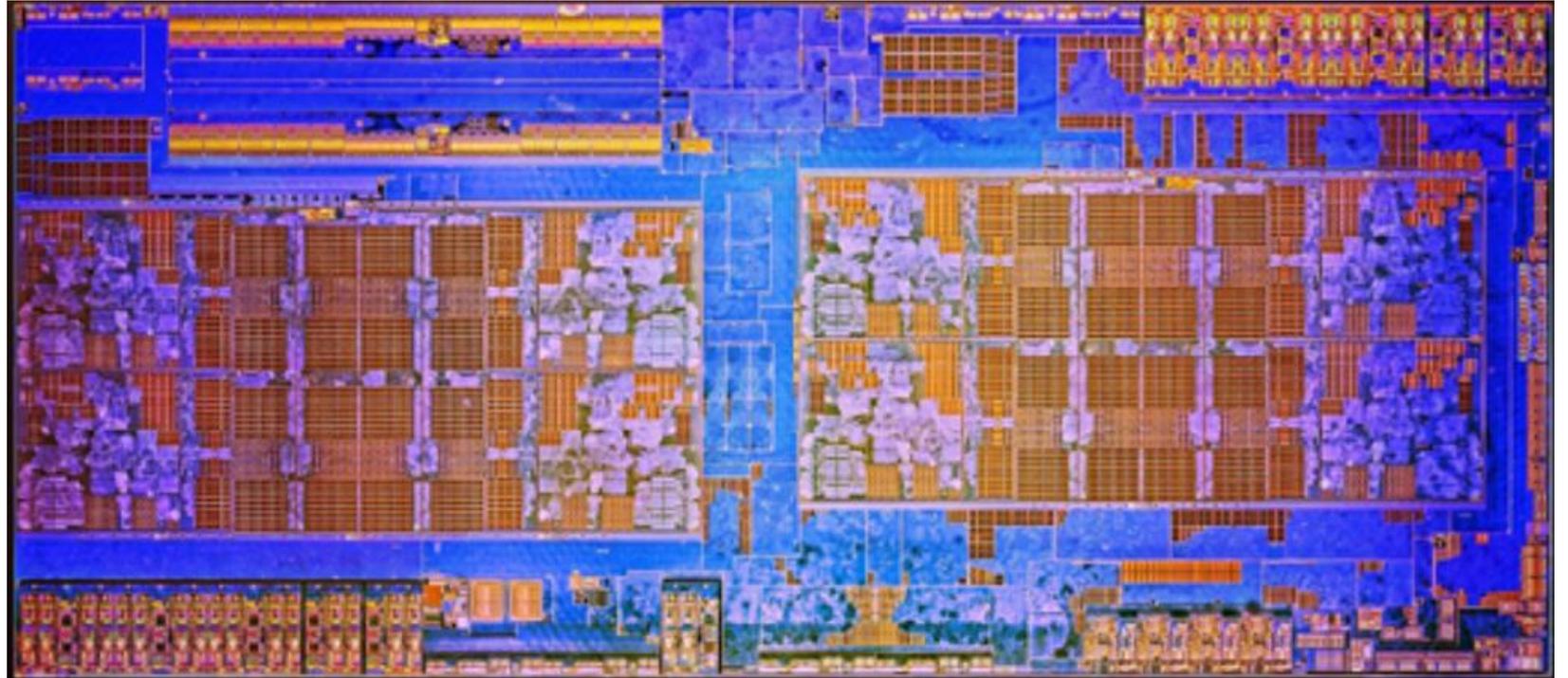
70 nm X-pitch,
60 nm Y-pitch



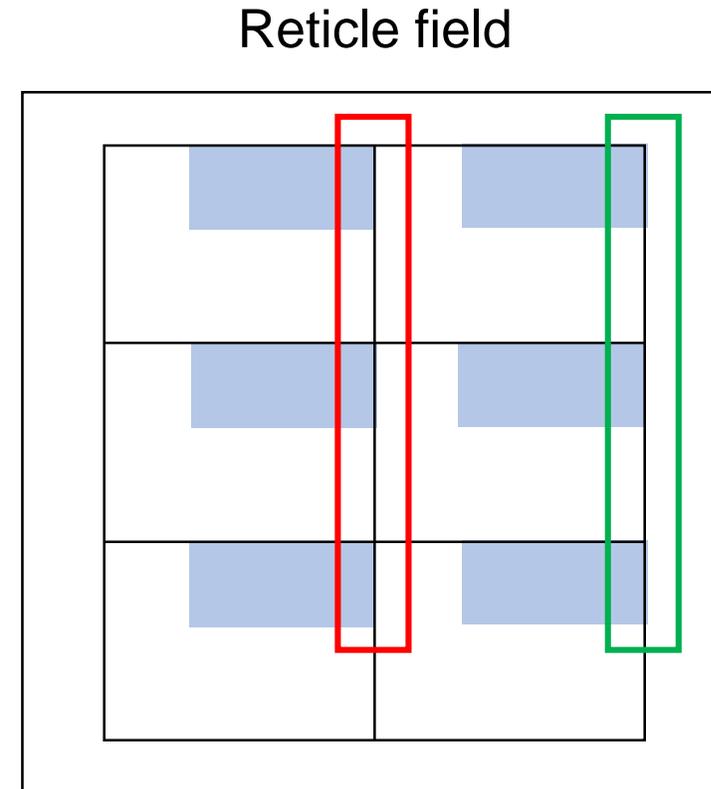
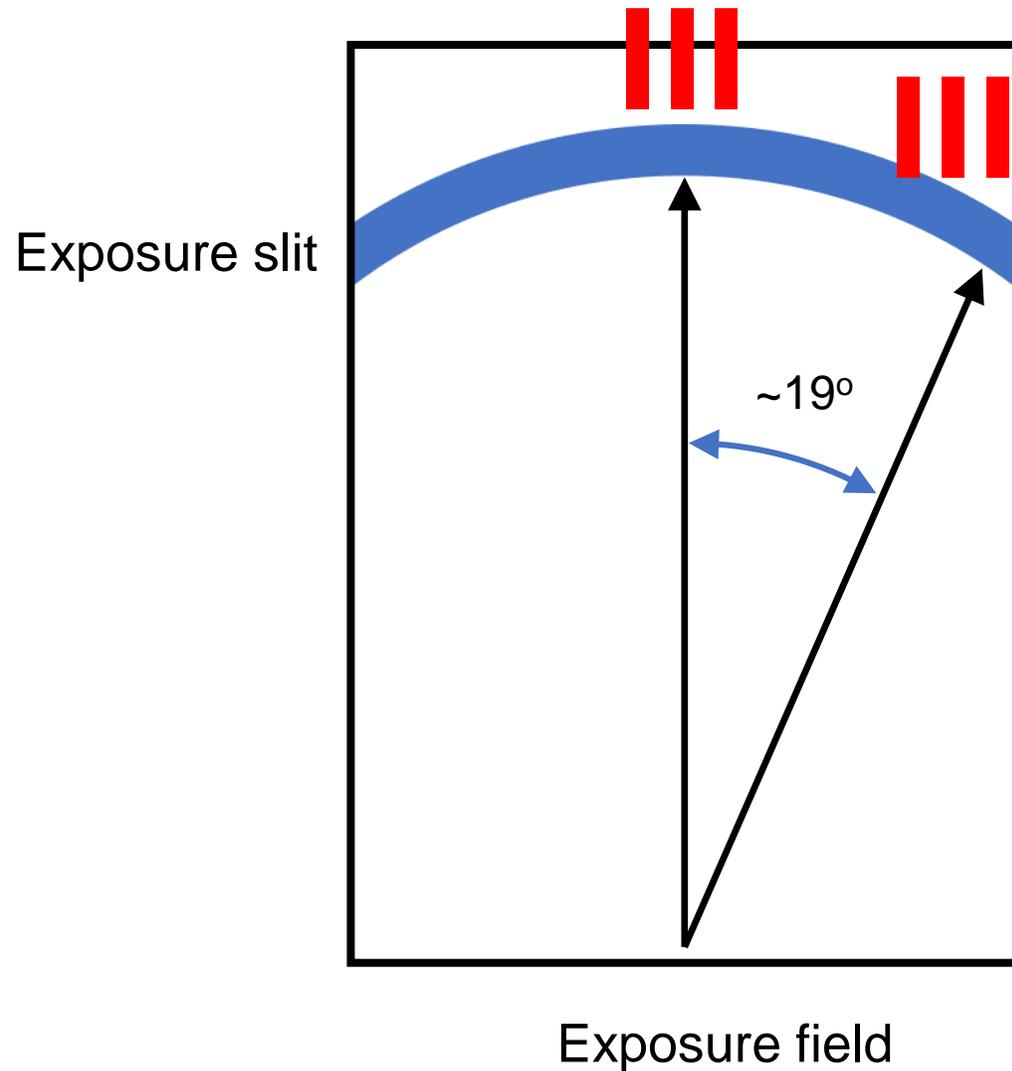
K. Hooker, A. Kazarian, X. Zhou, J. Tuttle, G. Xiao, Y. Zhang, and K. Lucas
"New methodologies for lower-K1 EUV OPC and RET optimization."
Proc. SPIE Vol. 10143 (2017)

Many geometries in today's chips creates big computational problem

- AMD's Ryzen 7 microprocessor has 4.8B transistors



Ring-field EUV optics kills hierarchy – another computation complexity



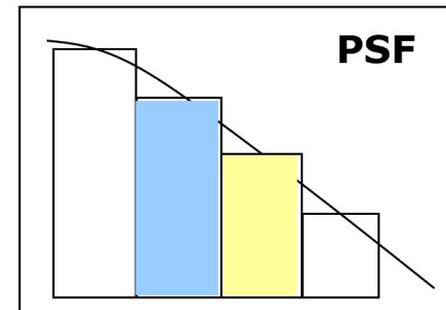
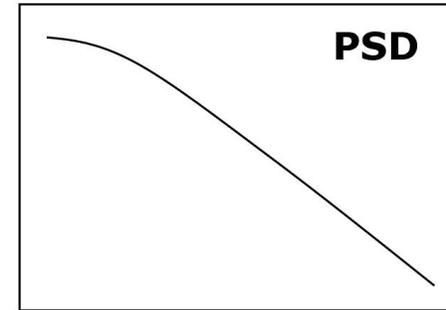
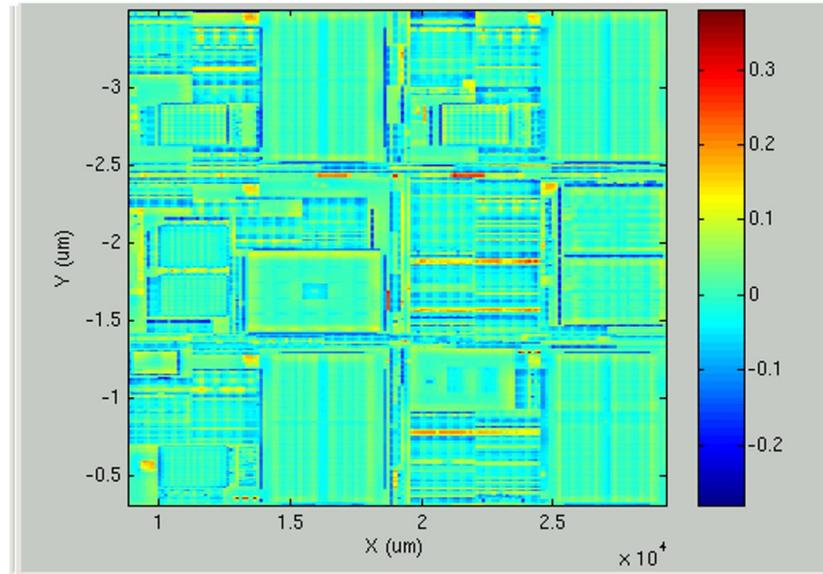
Flare also breaks hierarchy

OPC Development: flare compensation



- Based on optics PSD and mask pattern density calculations

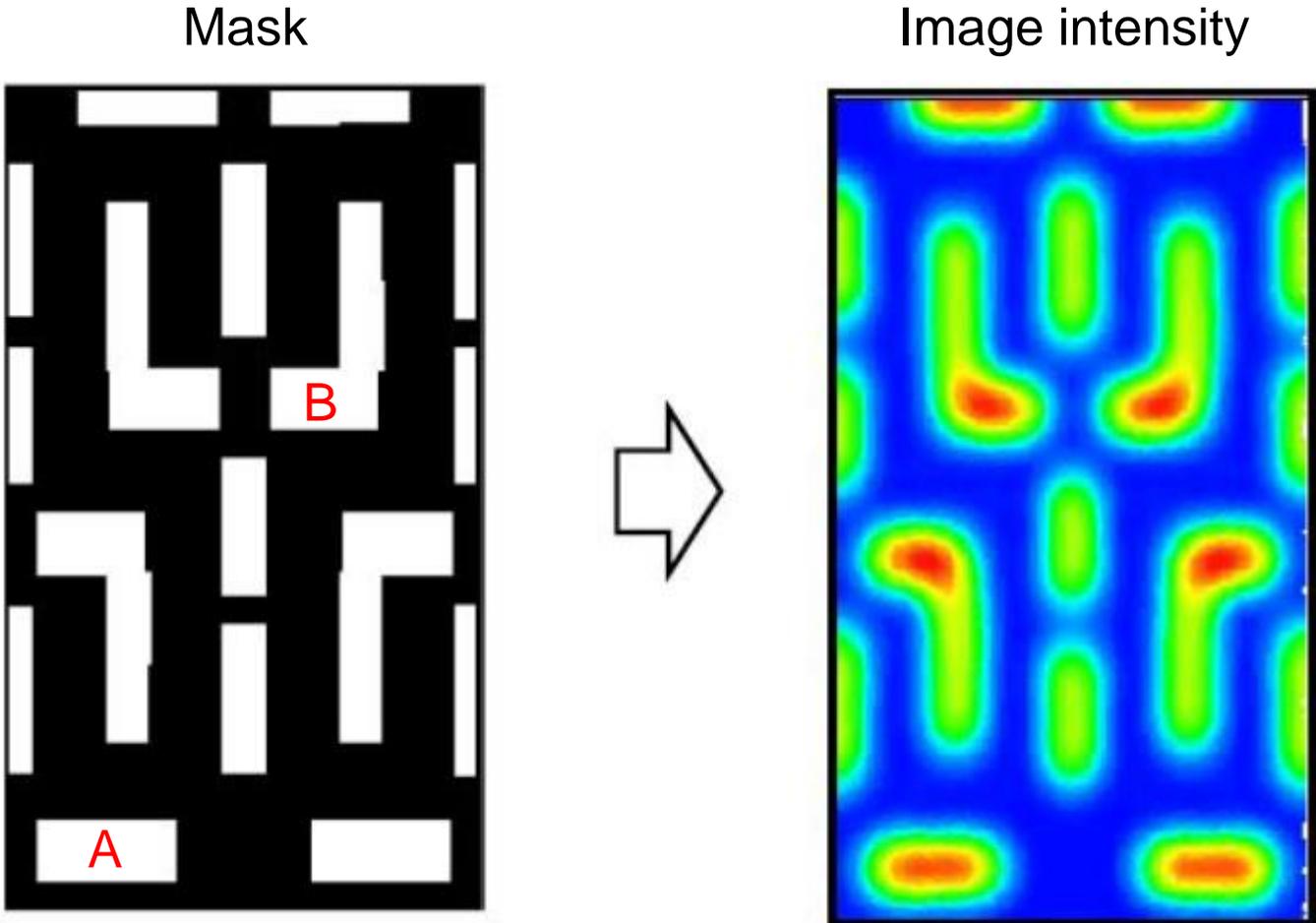
Long-range density effects



Current situation

- The physics of EUV lithography necessitates computations more complex than those encountered in optical lithography
 - Significant mask 3D effects
 - Multiple manifestations
 - Plane of best focus dependent on pitch and position within arrays
 - Image blur
 - Pattern placement shifts
 - Variations across the slit
 - Flare and aberrations
 - Complex resist behavior
- Support needed for curvilinear features
- Large chip sizes at the leading edge creates need for fast computational capabilities

Lithography simulations are amenable to parallel computations



P. De Bisschop,
JM3, 2018

Lithography simulations are amenable to parallel computations

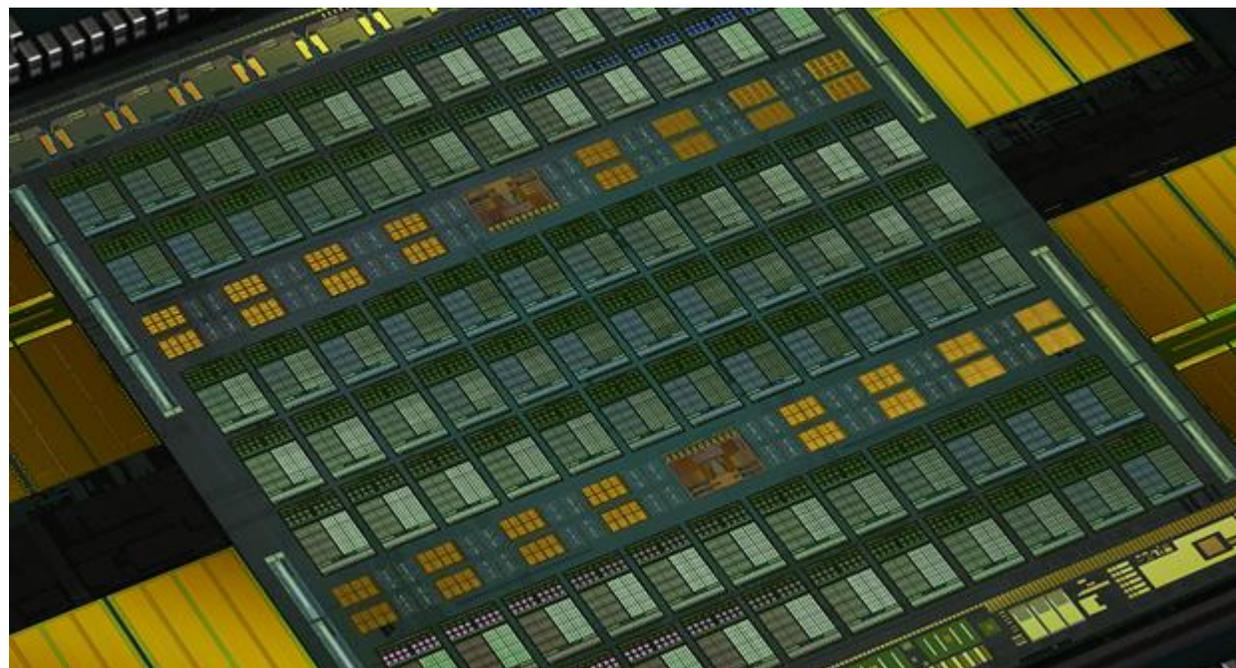
- Use of multiple servers with multiple-core processors are used routinely for optical lithography
- Example
 - 64 core microprocessors
 - 100 servers
 - 6400 cores
- OPC computations can still take 24 hours or more for optical lithography
- Inverse lithography calculations can take so long that they are often applied only to select patterns
- Greater computational capability will be needed for EUV lithography

Lithographic calculations extensively involve FFTs



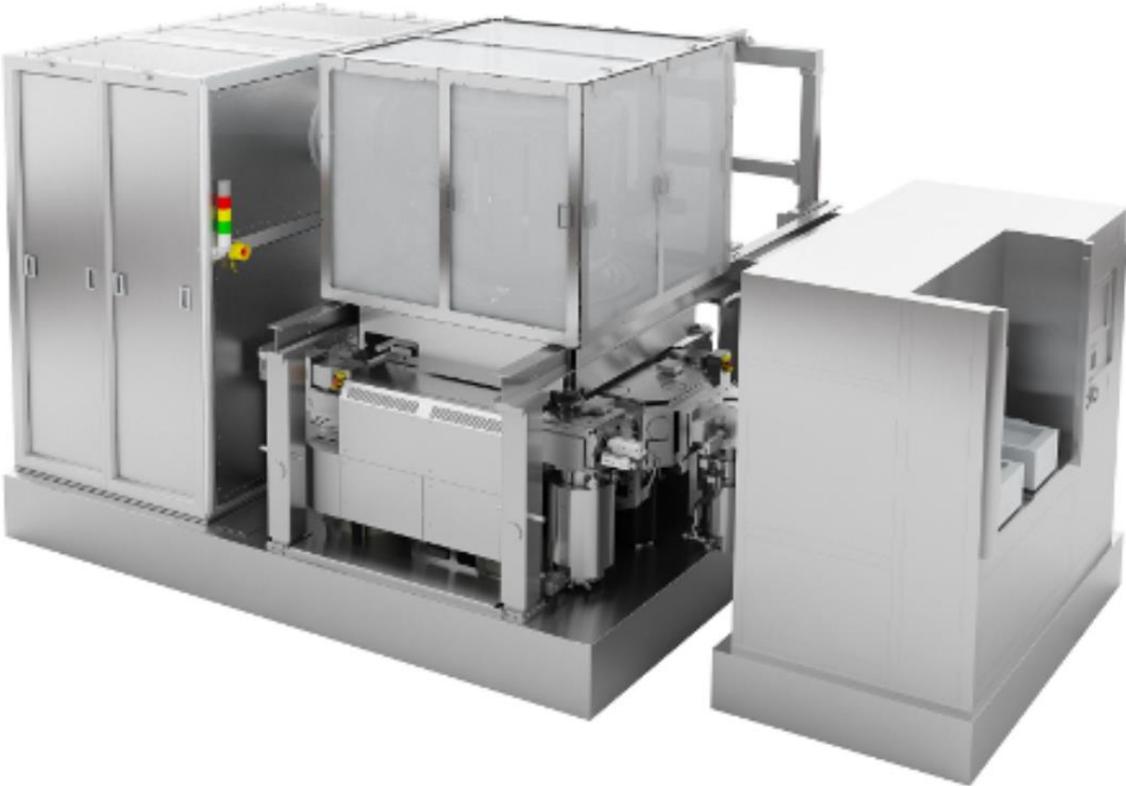
Parallel computations: New paradigm with GPUs

Nvidia Volta GPU:
5120 cores

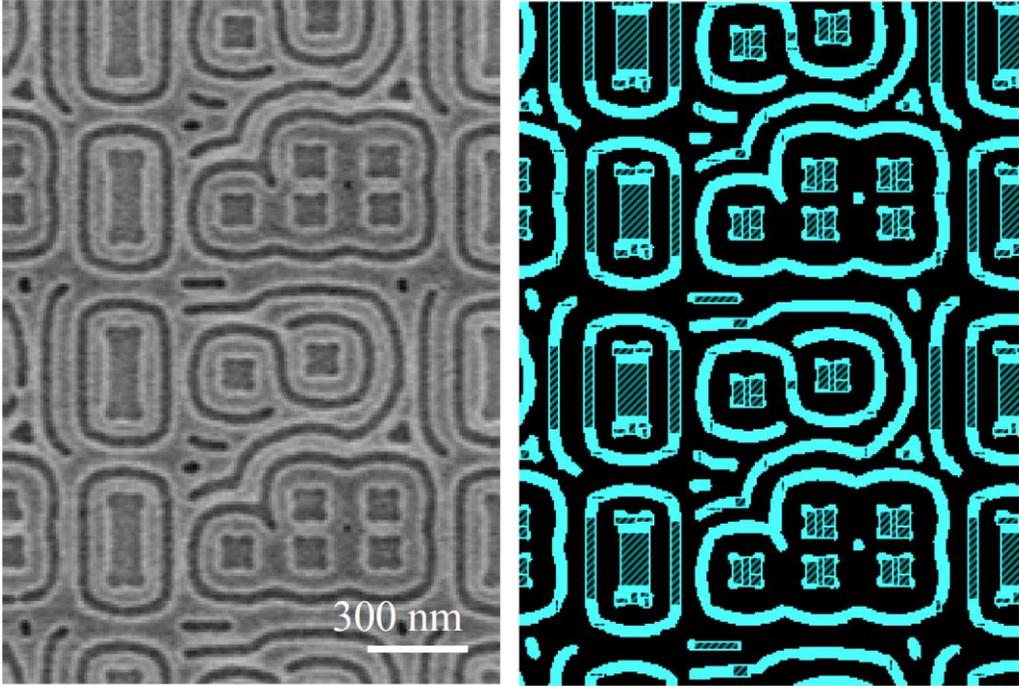


Curvilinear shapes: practical with multi-beam mask writing

Return to raster scanning



IMS MBMW-101



Patterns created with Nuflare MBM-1000

Summary

- Future OPC/RET for EUV lithography will necessarily be very complex
 - Mask 3D effects
 - Increases need for SRAFs
 - Resist physics
- Large chips manufactured with leading-edge lithography necessitate powerful computational and mask-making capabilities
- Fortunately, the infrastructure is becoming available to support solutions
 - GPU's can provide a path to a much higher degree of parallel computing
 - EUV exposure tools now have freeform pupil shaping capabilities
 - Multiple-beam mask writers enable curvilinear patterns