This is really a no-brainer …

What’s Happening and What’s the Meaning:

**ASML introduces AI to its product portfolio**: This is really a no-brainer. That said, the problem that most equipment companies have is finding good applications for it, as they find all they have is little data to feed the NN (more on that below). Anyway, this will be a good test for DLNNs as to whether engineers will accept results without knowing what’s in the ‘blackbox,’ which is a classic barrier to this technology. I believe they will because comparing results to input consistency are pretty easy to test out in this case. Especially since ASML led the way into computational lithography, albeit with plenty of customer pull.

Source: *The Chip Insider*® VLSIresearch
Machine learning brings revolution to many applications!

Can machine learning be the moonshot for us?
We have been doing machine learning for a long time … with manual feature engineering

Machine Learning

Input → Feature extraction → Classification → Output

Mask layout → Optical model design → Optical kernels → Aerial image

Aerial image → Resist model design → Resist kernels → Resist contour

Few hidden layers = Shallow neural network

1: E. Abbe, H. H. Hopkins
2: F. H. Dill, C. Mack
Machine Learning evolved to Deep Learning
Less human intervention in growing data volume analysis

Massive metrology data & deep learning models further improve OPC accuracy in customer case

- Big data improve pattern coverage & enhance model accuracy
- Deep Learning Model has more benefits with big data vs Traditional Model

Source: Jeff Dean, Google, “Trends and developments in deep learning”, Jan’17
High speed e-beam metrology and large field of view

Excellent precision across large field of view

Metrology Throughput advantage over CD-SEM

<table>
<thead>
<tr>
<th></th>
<th>CD-SEM</th>
<th>eP5</th>
<th>68</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>1 nm</td>
<td>1 nm</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>8 pA</td>
<td>250 pA</td>
<td></td>
</tr>
<tr>
<td>Scan Rate</td>
<td>16 MHz</td>
<td>100 MHz</td>
<td></td>
</tr>
<tr>
<td>Field of view</td>
<td>1 um</td>
<td>12 um</td>
<td></td>
</tr>
</tbody>
</table>

Throughput

12

1

CD-SEM (1um FOV)  eP5 (1um FOV)  eP5 (12um FOV)
Improving OPC model accuracy by 2X on DRAM enabled by deep learning, fast e-beam, and metrology processing

Model prediction error (RMS) validated with >150k Edge Placement (EP) Gauges

-32%
  • Systematic error removal
  • Random noise reduction
  • Improved pattern coverage

-18%
  • Capture unknown physical effects

Baseline metrology
w/o deep learning
(CD gauges)

~18 hours
Metrology collection time

eP5-MXP
w/o deep learning
3.3x (CD+EP gauges)

~3 hours
Metrology collection time
3x images

eP5-MXP
with deep learning
3.3x (CD+EP gauges)

Deep learning resist model
Improve OPC model accuracy

OPC Model accuracy study using high volume contour based gauges and deep learning on memory device, Young-Seok Kim et al., SPIE 2019, 10959-37
Better accuracy of lithography models by deep learning
Enabled by fast e-beam metrology and physical based models

Physical driven **training** using physics based lithography models

- Physical Resist Shrinkage
- Resist surface stress
- Data expansion through simulated contours

Data-driven **training** based on fitting spec and wafer measurements

- Large volume wafer metrology data, further enhanced by fast e-beam

---

**Model Prediction Accuracy (RMS in nm)**

**EUV Cases: 7 nm and 5 nm logic**

<table>
<thead>
<tr>
<th></th>
<th>1D</th>
<th>2D</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ASML Deep Learning model</strong></td>
<td>0.7</td>
<td>0.4</td>
</tr>
<tr>
<td><strong>with Deep Learning</strong></td>
<td>0.34</td>
<td>0.32</td>
</tr>
<tr>
<td><strong>without Deep Learning</strong></td>
<td>1.0</td>
<td>0.7</td>
</tr>
</tbody>
</table>

**DUV Cases: 7 nm and 5 nm logic**

<table>
<thead>
<tr>
<th></th>
<th>EP SET1</th>
<th>EP SET2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ASML Deep Learning model</strong></td>
<td>1.1</td>
<td>1.2</td>
</tr>
<tr>
<td><strong>with Deep Learning</strong></td>
<td>0.7</td>
<td>0.4</td>
</tr>
<tr>
<td><strong>without Deep Learning</strong></td>
<td>1.3</td>
<td>1.0</td>
</tr>
</tbody>
</table>

---

"EP SET1" → Edge Placement Gauge Set 1
“Moore’s Law” of Computational Lithography
Runtime and cost of OPC increases node-by-node

<table>
<thead>
<tr>
<th>Technology Node</th>
<th>28nm</th>
<th>22nm</th>
<th>14nm</th>
<th>10nm</th>
<th>7nm</th>
<th>5nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Production start</td>
<td>2011</td>
<td>2013</td>
<td>2014</td>
<td>2016</td>
<td>2017</td>
<td>2019</td>
</tr>
<tr>
<td>Average transistor density (billion/cm²)</td>
<td>1.17</td>
<td>1.63</td>
<td>2.34</td>
<td>3.75</td>
<td>6.25</td>
<td>10.71</td>
</tr>
<tr>
<td>Number of critical layer masks</td>
<td>18</td>
<td>24</td>
<td>33</td>
<td>37</td>
<td>47</td>
<td>66</td>
</tr>
<tr>
<td>Normalized OPC runtime per layer per unit area</td>
<td>1</td>
<td>1.4</td>
<td>2</td>
<td>2.7</td>
<td>4</td>
<td>5.6</td>
</tr>
</tbody>
</table>

**Node-on-node OPC runtime trends**

**Worldwide comp litho total capacity**

Total computational litho capacity worldwide on the order of 10 petaflops
Deep learning inverse model speeds up full-chip OPC by providing a good starting point

Selected clips

Design target

Inverse mask image

Complex, Iterative Optimization

Training input

Deep Learning Inverse Model

Training on clips

Inference on full chip

Full chip layout

Design target

Inverse mask image

Deep Learning Inverse Model

Full chip layout (Post-OPC)
Improving training pattern coverage using machine-learning-based pattern selection

Full-chip Layout  →  Pattern Library  →  Machine-learning-based pattern selection  →  Training Pattern Set

Feature Generation → Pattern Clustering → Representative Selection

Normalized RMS between prediction and ground-truth (inverse solution)

Critical PV-band (>15% CD error) Comparison

Full-chip application of machine learning SRAFs on DRAM case using auto pattern selection  K. Chen et al., SPIE 2019, 10961-37
Deep learning SRAF improves full-chip DoF by 24% for DRAM contact hole layer, validated on wafer

Newron SRAF places more accurate assist features to remove the process window limiter

Newron SRAF wafer validation shows 24% DoF improvement

Baseline solution (Rule-Based SRAF)

Newron SRAF (Deep Learning)

Baseline solution (Rule-Based SRAF)

Newron SRAF (Deep Learning)

Full-chip application of machine learning SRAFs on DRAM case using auto pattern selection  
K. Chen et al., SPIE 2019, 10961-37
Leverage confluence of new technologies to meet OPC technology and cost requirements

<table>
<thead>
<tr>
<th>Year</th>
<th>2016</th>
<th>2017</th>
<th>2018</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ASML</strong></td>
<td><img src="image" alt="Inverse OPC (CTM)" /></td>
<td><img src="image" alt="Intel Xeon® Processor ES v4" /></td>
<td><img src="image" alt="Intel Xeon® Platinum" /></td>
<td><img src="image" alt="Intel Xeon® Platinum (CTM+)" /></td>
<td><img src="image" alt="Intel Xeon® Platinum" /></td>
<td><img src="image" alt="Intel Xeon® Platinum" /></td>
</tr>
<tr>
<td>Mask writer &amp; inspection</td>
<td><img src="image" alt="Multi-beam Mask Writer available" /></td>
<td><img src="image" alt="Mask inspection available" /></td>
<td><img src="image" alt="Mask making infrastructure is ready for inverse OPC &amp; curvi-linear masks" /></td>
<td><img src="image" alt="Intel DL Boost" /></td>
<td><img src="image" alt="Hardware Accel. (tentative)" /></td>
<td><img src="image" alt="Next Gen?" /></td>
</tr>
<tr>
<td><strong>Intel</strong></td>
<td><img src="image" alt="Inverse OPC (CTM)" /></td>
<td><img src="image" alt="Intel Xeon® Platinum" /></td>
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</tr>
<tr>
<td><strong>NVIDIA</strong></td>
<td><img src="image" alt="Pascal" /></td>
<td><img src="image" alt="Volta" /></td>
<td><img src="image" alt="Turing" /></td>
<td><img src="image" alt="Next Gen?" /></td>
<td><img src="image" alt="Next Gen?" /></td>
<td><img src="image" alt="Next Gen?" /></td>
</tr>
</tbody>
</table>

**ASML**

- Mask writer & inspection
  - Multi-beam Mask Writer available
  - Mask inspection available

**Intel**

- Inverse OPC (CTM)
- Multi-beam Mask Writer available
- Inverse with phase control
- Hardware Accel. (tentative)

**NVIDIA**

- Pascal
- Volta
- Turing
- Next Gen?
Context-aware control extends holistic solutions.

Context Data

Litho InSight and Pattern Fidelity Enhancements
Leveling, Alignment, Metrology Overlay, Focus, pattern defect control and scanner/etcher co-optimization

Corrections

Metrology design & setup
Model, sampling & control setup
Monitoring & analytics
Leverage machine learning to address wafer-to-wafer variation induced by different wafer process routes.

A novel patterning control strategy based on real-time fingerprint recognition and adaptive wafer level scanner optimization.

H. E. Hakli et al., SPIE 2018, 10585:105851N

ASML Machine Learning Model

Overlay Variations

Correlate wafer-to-wafer variation to process context and apply run-to-run control with context-based grouping.

Context based Overlay Control results

Wafers in spec

(225 wafers processed)

100%

95%
Predict dense alignment from dense leveling data hybrid metrology enabled by machine learning

**Known input**
- Leveling & Alignment all wafers
- Overlay or alignment sampling from same wafer (blue points)

**Prediction**
- Unknown (orange points)
- Overlay or alignment from same wafer at different coordinate locations

**Machine Learning**

Pairing wafer leveling metrology from a lithographic apparatus with deep learning to enable cost effective dense wafer alignment metrology

E. Schmitt-Weaver & K. Bhattacharyya, SPIE 2019, 10961-7
Holistic Lithography delivering significant customer value

Lithography scanner with advanced control capability

Applications
Patterning Control

Algorithms
Physical Models, Optimization, Machine Learning

Data
Scatterometry, SEM, & other fab equipment

Optical and e-beam metrology

Etch and deposition tools

Computational lithography and metrology
Major trends in semiconductor-enabled computing:

- **Autonomous decisions**
- **Immersive experience**

Moore’s Law:

- **Applications**
- **Performance**
- **Cost**

Data → Value
Deep Learning

Data

Connectivity
Real-time
Volume