

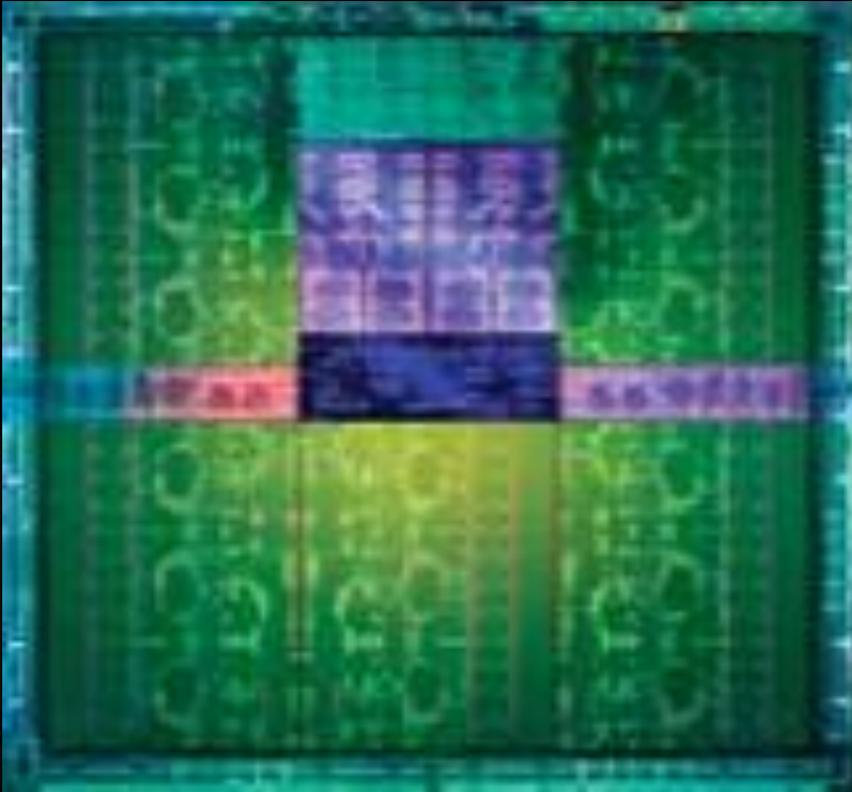


2013 Bacus  
Monterey, Sept

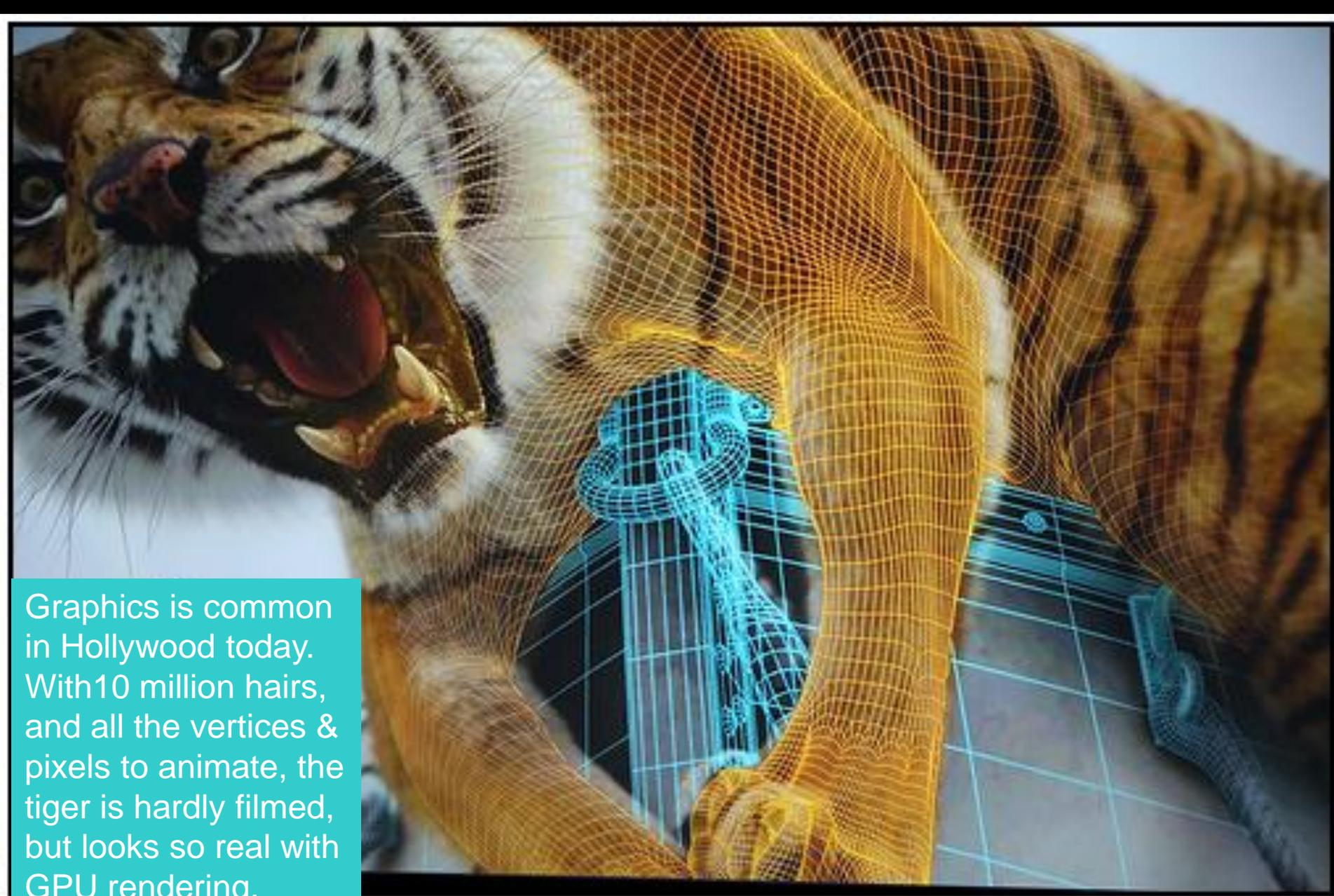
*From lines and spaces to patterns and shapes*

**John Y. Chen**

# Kepler GK110, a high performance chip for graphics and computing



- 2048 SM cores  
made by 28nm  
Hk/MG tech
- 7.1B X'tors
- 19.7B contacts +  
20.5B via's + 20Km  
1x metal lines
- 553 mm<sup>2</sup>



Graphics is common in Hollywood today. With 10 million hairs, and all the vertices & pixels to animate, the tiger is hardly filmed, but looks so real with GPU rendering.

*Jen-Hsun Huang's keynote at 2013 GPC*

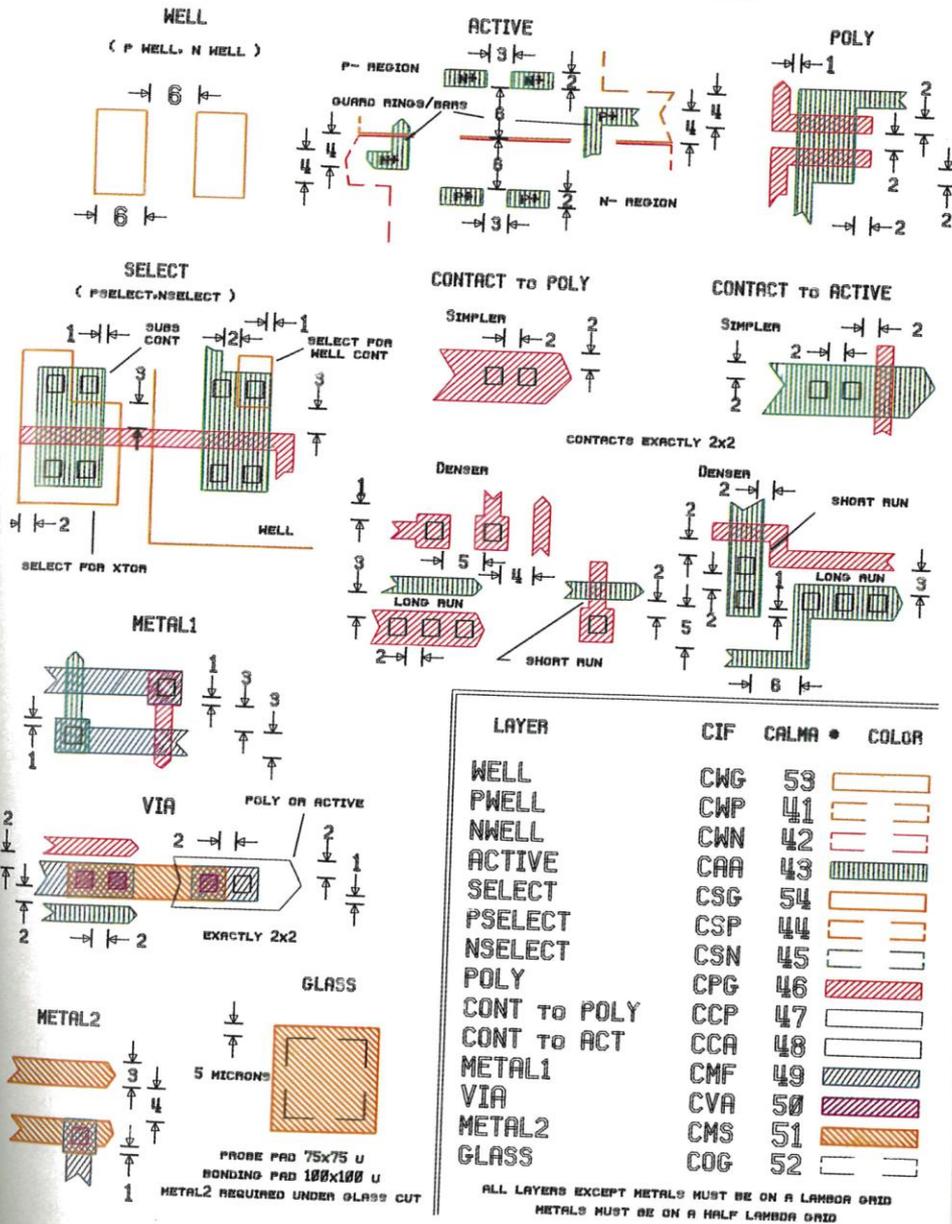
*Showing off a digital tiger generated for 'Life of Pi' by Rhythm and Hues.*

# Graphics vs. Mask making

<u>Graphics</u>	<u>Mask making</u>
<b>Vertices, Lines, &amp; Triangles</b>	<b>Lines, spaces &amp; rectangles</b>
<b>Geometries</b>	<b>Shapes</b>
<b>Pixel shading</b>	<b>Dose and Contrast</b>
<b>Photo realism</b>	<b>Pattern replication</b>

**Both deal with images with huge data base**

# MOSIS CMOS SCALABLE RULES



LAYER	CIF	CALMA •	COLOR
WELL	CWG	53	
PWELL	CWP	41	
NWELL	CWN	42	
ACTIVE	CAA	43	
SELECT	CSG	54	
PSELECT	CSP	44	
NSELECT	CSN	45	
POLY	CPG	46	
CONT TO POLY	CCP	47	
CONT TO ACT	CCA	48	
METAL1	CMF	49	
VIA	CVA	50	
METAL2	CMS	51	
GLASS	COG	52	

ALL LAYERS EXCEPT METALS MUST BE ON A LAMBDA GRID  
METALS MUST BE ON A HALF LAMBDA GRID

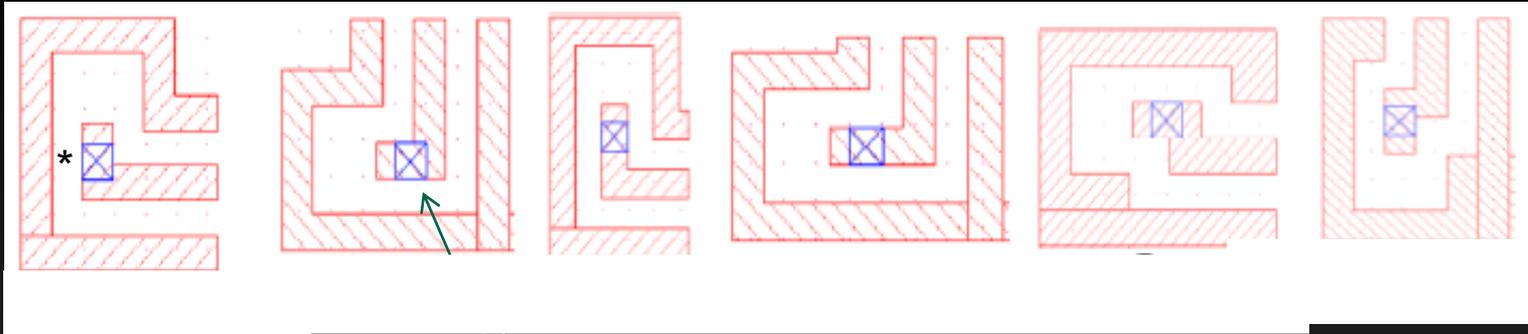
**MOSIS offering in the 80's**

**Scalable Design Rules drawn by unit of  $\lambda$ , ( $\lambda$  scales w/ technology node)**

**All lines/spaces on one page**

John Y. Chen, "CMOS Devices and Technology for VLSI," Prentice Hall, 1990.

# L-shape metal pattern with via above



## Via Layout:

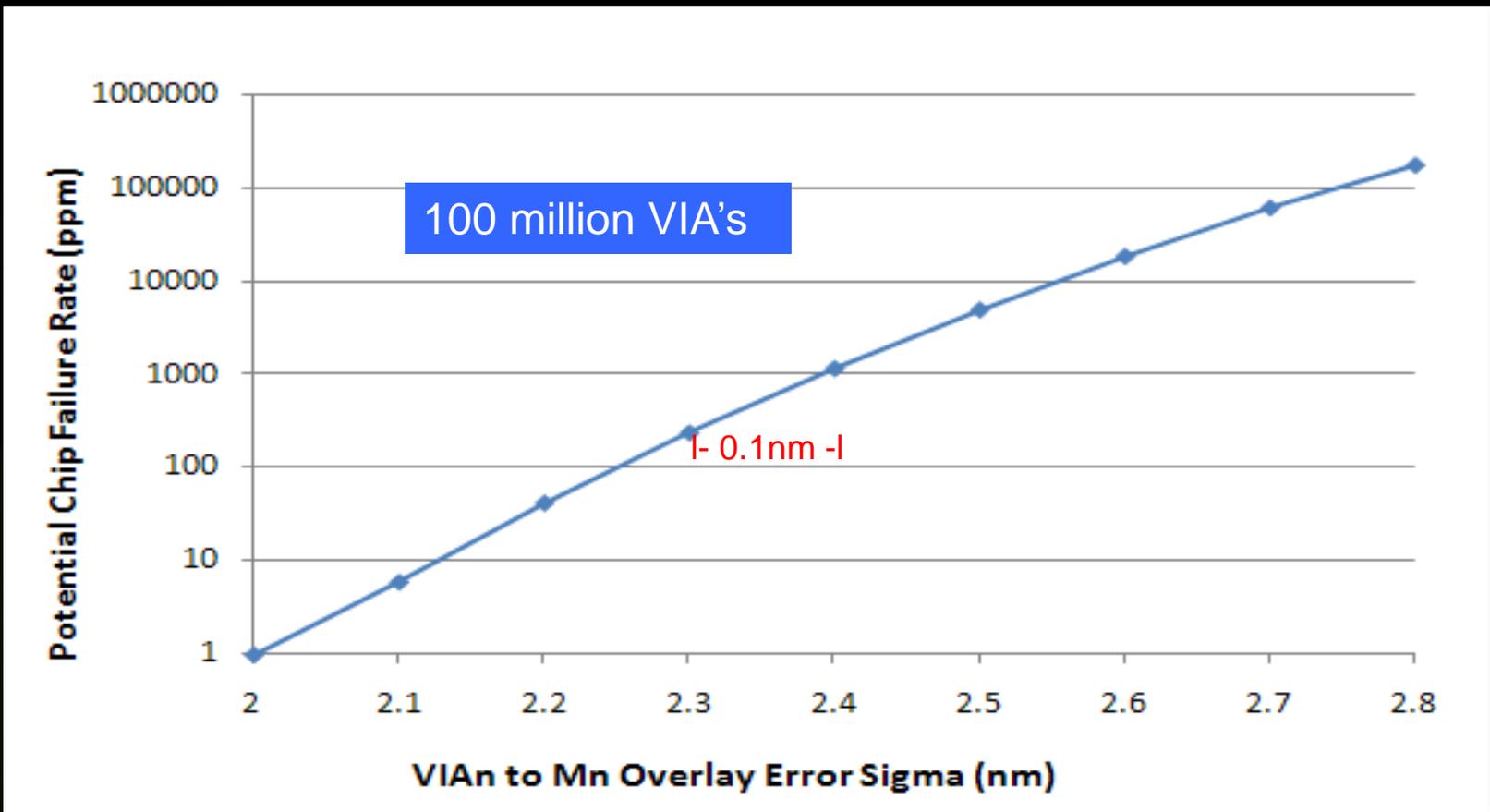
- L shaped underlying metal line
- 0/min enclosure on x/y
- 4 corners with another surrounding metal -> OPC unfriendly
- DFM down to 1% for this type

## Process control:

- Precise Litho
- Etch with min  $\mu$ -loading
- Perfect Cu fill

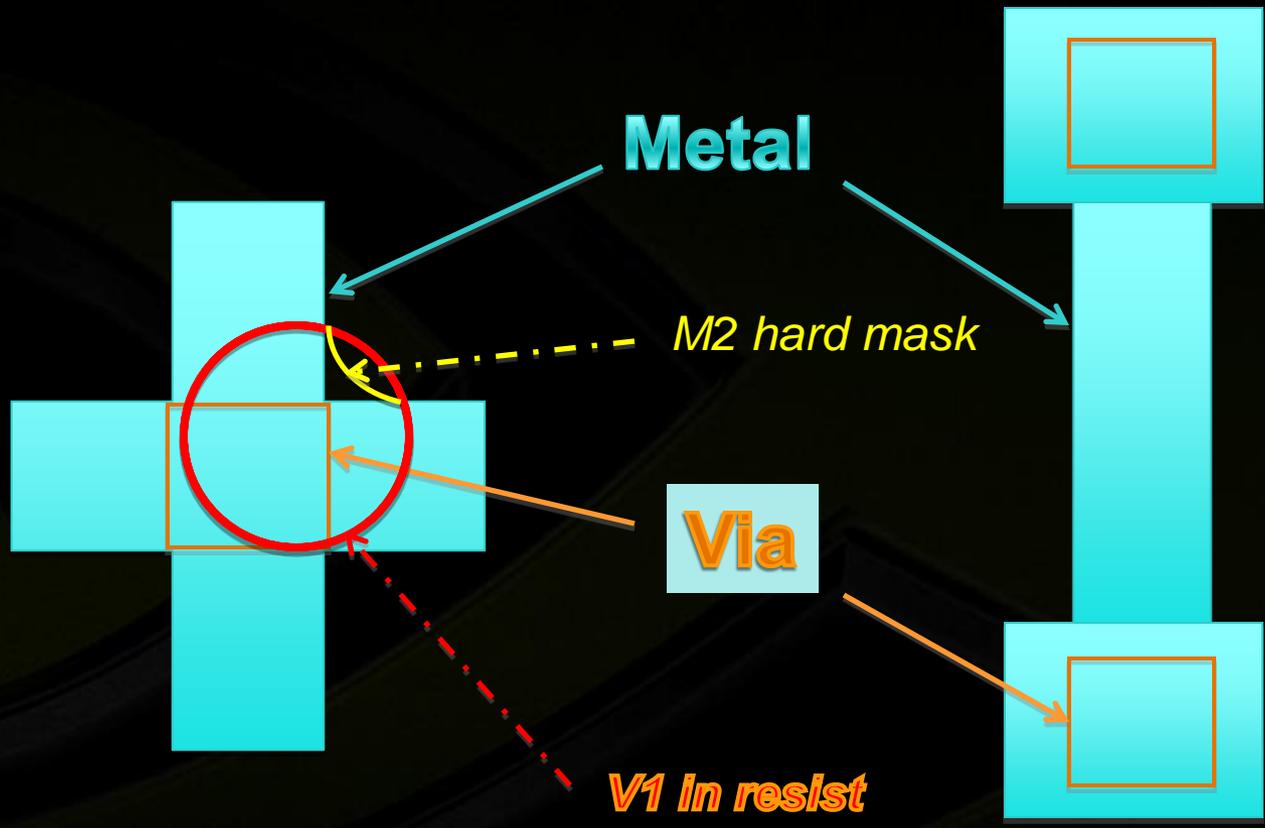
- ***To guarantee the min space needed for TDDB Reliability, how tight the control needs to be ?***

# Control down to 0.1nm, every tenth nm counts!



32nm drawn rule for min Mn and VIAN in a 20nm design

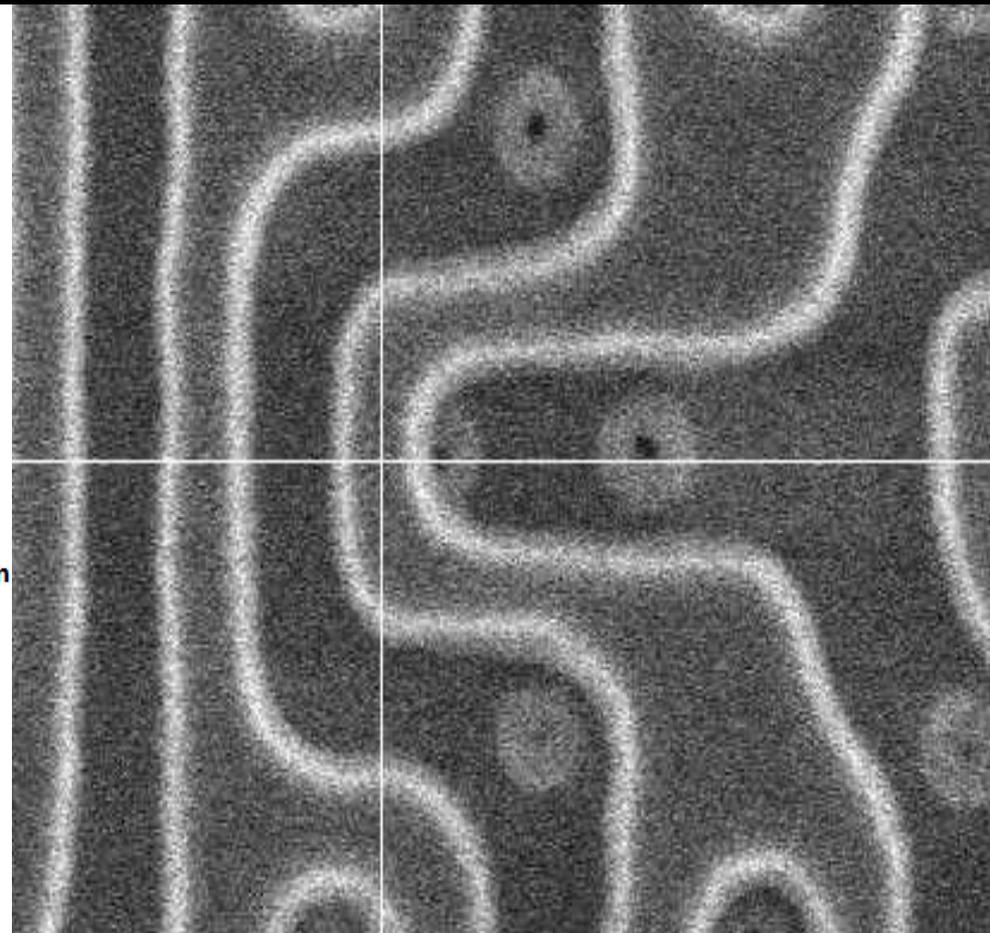
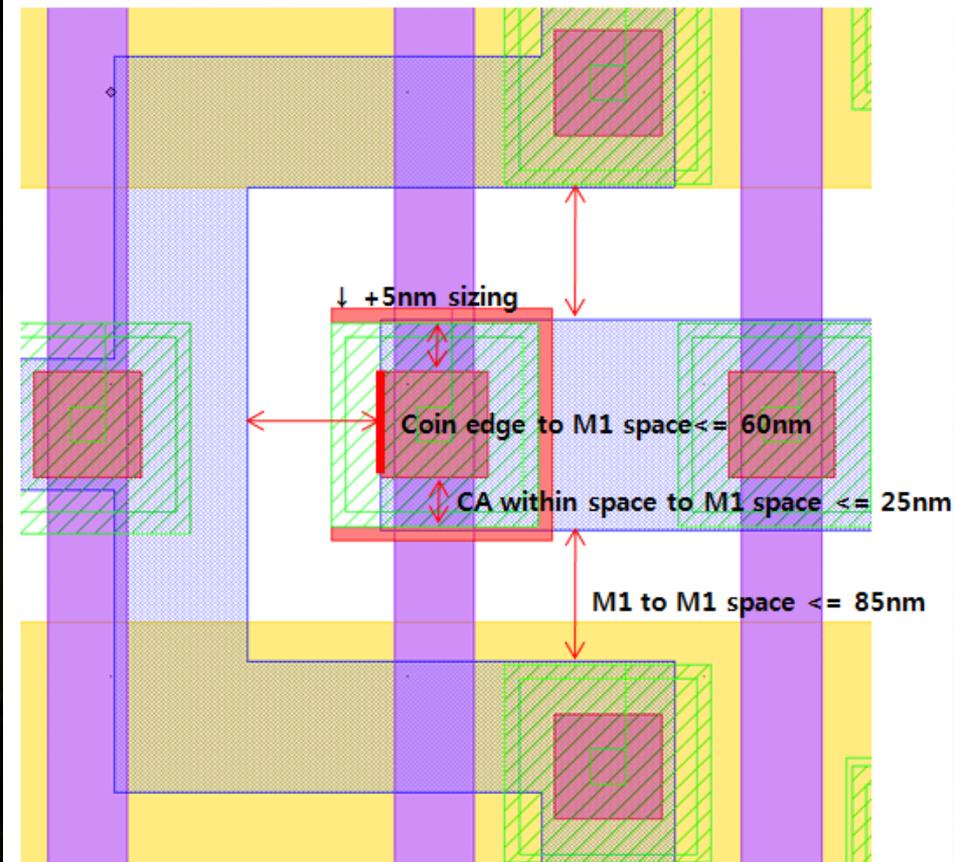
# Crosses and Dogbones



# E-shape metal over contact



## CA on the line end of the M1

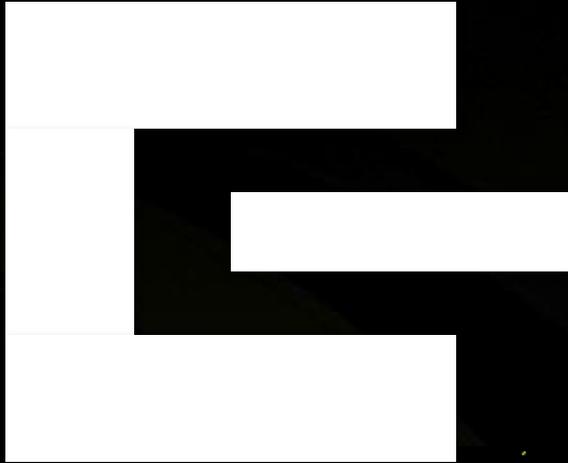


# The E-shape metal

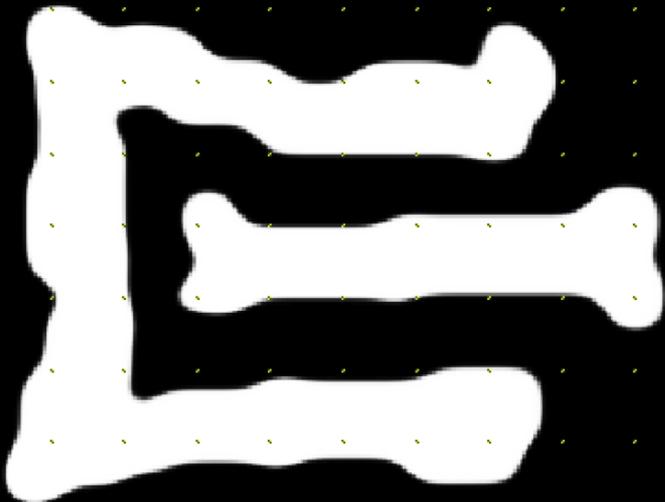


- Margins gained by using ILT w/MB-MDP (Model Based Mask Data Preparation)

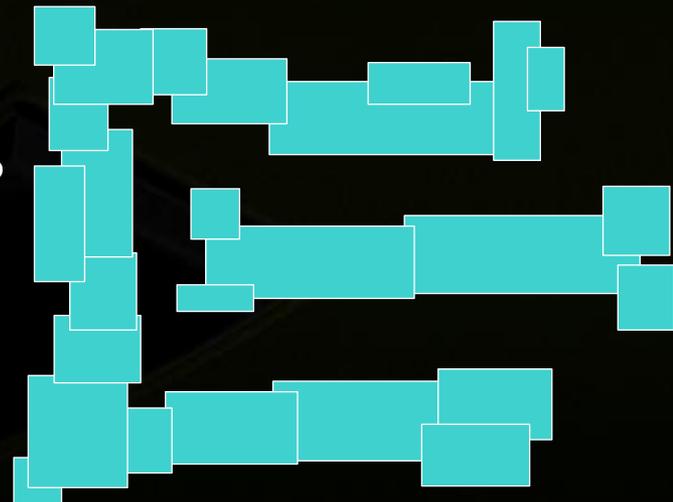
DESIGN

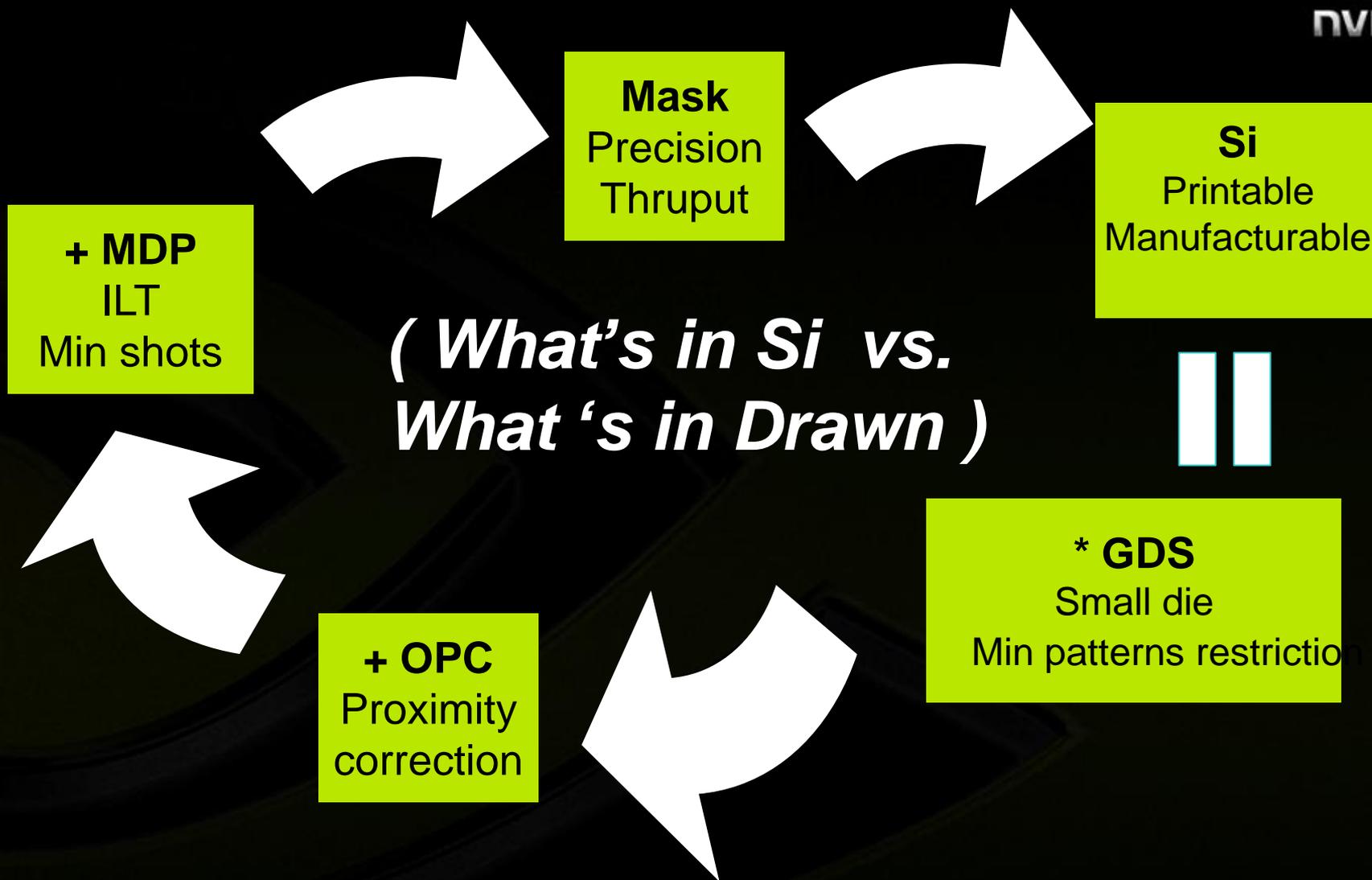


ILT



MB-MDP  
Shots





# Accelerated Computing

## Multi-core plus Many-cores

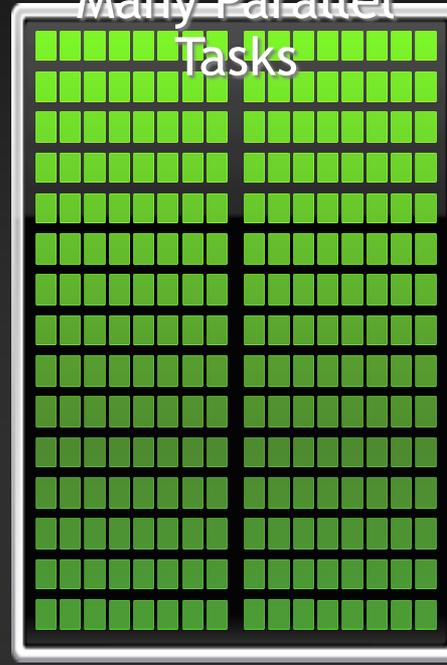
**CPU**

Optimized for  
Serial Tasks



**GPU**

**Accelerator**  
Optimized for  
Many Parallel  
Tasks



10x Performance  
5x Energy Efficiency

