Curvilinear Masks in Memory Designs: From DUV to EUV

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Outline

- Enabling DRAM and NAND scaling roadmaps
- A case for curvilinear masks to extend DUV multi-patterning
- EUV curvilinear masks need
  - A DRAM array example
- Conclusions
### Scaling Challenges

Advanced technology nodes face increasingly complex and disruptive scaling challenges

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<td>Cost scaling and accelerated performance improvements required</td>
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**EUV, multi-patterning**

- 110nm
- 90nm
- 70 to 40nm
- 3x to 1znm
- Beyond

**64-tier, 128-tier, 176-tier**
Micron Roadmaps beyond 1-alpha and 176 layers

**DRAM**
- **2021**
  - Shipped industry’s first 1α DRAM process technology
- **2022**
  - World’s first 176-layer NAND

**NAND**
- **2021**
  - Expanded 176-layer NAND across TLC and QLC SSD portfolio
- **2022**
  - World’s first 176-layer NAND

**2XX** Manufacturing CY2022
**1β** Manufacturing CY2022

**1γ** Development

**1δ/ε** Pathfinding

**2YY** Development

**Next Gen** Pathfinding
Micron’s pattern multiplication is a strategic advantage

June 2021 Micron announced EUV adoption for advanced nodes in development

Continue to extend DUV multi-patterning in advanced DRAM and NAND nodes
1-alpha DRAM and 176-layer 3DNAND
- Using optical multi-patterning lithography
- Extend RET and OPC techniques to extract achieve process window

Enablers
- ILT: Curvilinear and stepped-Manhattan masks
- Model-based retargeting → Curvy designs
- Efficient use (and reconstruction) of hierarchy for manageable cycle time for ILT
Why Curvilinear Masks

- **More degrees of freedom for OPC solutions**
  - *Assist features*: improved process window, optimal placement
  - *Main features*: infinitesimally small segmentation of OPC, higher degree of control of the correction
  - Physically meaningful MRCs (no corner-to-corner)
  - Accurate target representation for Mask and Wafer

- **Mask Fidelity**
  - Improved matching between mask and intended OPC shapes
  - More accurate OPC models
    - No need to compensate for differences between “intended” shape and mask shape
  - Mask friendly shapes (no sharp corners)
    - Mask uniformity: reduces variations at feature corners
Curvilinear Masks: DRAM Array Layer

- Curvilinear DRAM Array shapes produced visually more consistent shapes
- Wafer CD Uniformity shows a ~10% improvement for curvilinear mask

CD Variation

Wafer CD
(through dose and mask bias)
Application of ILT and Curvilinear Masks

- **ILT is the ultimate OPC algorithm**
  - Starts from the intended wafer image to calculate the mask to produce that image
  - Naturally includes assist features
  - Pixel based solution, intrinsically curvilinear

- **ILT OPC improves process window and accuracy**
  - Optimal assist feature placement
  - Increased accuracy: solution is calculated in every point, not just few evaluation points
  - Computationally intensive: full-chip processing times were prohibitive
  - Curvilinear masks had to be approximated by stepped polygons to write them (Manhattanization)

- **Enablers today:**
  - Higher computation bandwidth: GPUs and faster CPUs
  - Multi-beam mask writers make full curvilinear masks possible
DRAM Array Core: Curvilinear ILT Correction

Improved NILS, CD Uniformity, and Contact Shape

Full-Chip ILT
- Application to a common DRAM array contact-like layer
  - CD uniformity and contact shape is critical

Mask Complexity
- Both Main features and assist features are curvilinear (small step Manhattanized) ILT

Memory Array Core

Assist Features (SRAFs)
ILT and Conventional OPC Blended

3D-NAND Routing Layer

- Leverage highly repeated areas using hierarchy reconstruction
  1. ILT correction in these areas \( \rightarrow \) Maximum PW
  2. Conventional OPC in other regions
  3. Blend solutions
3D-NAND Multi-Patterning Routing Layer

- ILT solution provides ideal assist-features
- Curvilinear output provides higher degree of freedom

- Tighter PV-Band
- Enhanced process window and edge placement
Curvilinear EUV Masks Need
A case for Curvilinear EUV Masks

Typical 3x2F DRAM cell architecture

Image from EDN magazine
A case for Curvilinear EUV Masks

- EUV used in next DRAM nodes to pattern critical layers

- Leverage higher EUV resolution now
  - DRAM array: Maximize cell contact and device performance
  - More complex target shapes to maximize to make use of available area
  - Define target as real wafer desired target to apply EUV-OPC

- Multi-beam writer required / Challenges:
  - Large data volume
  - How to efficiently apply MPC to incoming?
    - High data density
    - Flattened field data due to EUV OPC
  - Standard file format for Curvy data
EUV Curvilinear Optimization Flow

- Benefits
  - Ideal shape on wafer
  - Unconstrained ILT solution
  - Maximum process window
Conclusions

- Case for curvilinear masks and unconstrained OPC as an enabler to extend DUV multi-patterning
- Curvilinear mask shapes improve OPC model accuracy and help achieve a more uniform mask
- EUV curvilinear masks can be used to extend 0.33NA EUV tools but also to capitalize on additional resolution to pattern more complex shapes to improve memory design and performance
- Multi-beam writers required for large scale curvilinear mask
  - Infrastructure needs to be advanced for supporting a full curvilinear tapeout flow