SPIE ALP 2026 eBeam Initiative Luncheon Aki Fujimura, CEO, D2S, Inc.

Only Entirely Curvilinear Masks are Entirely Manufacturable Masks

1982-1985

Everything was analog

Thriller (1982), Epic Records. Cover photo by Dick Zimmerman

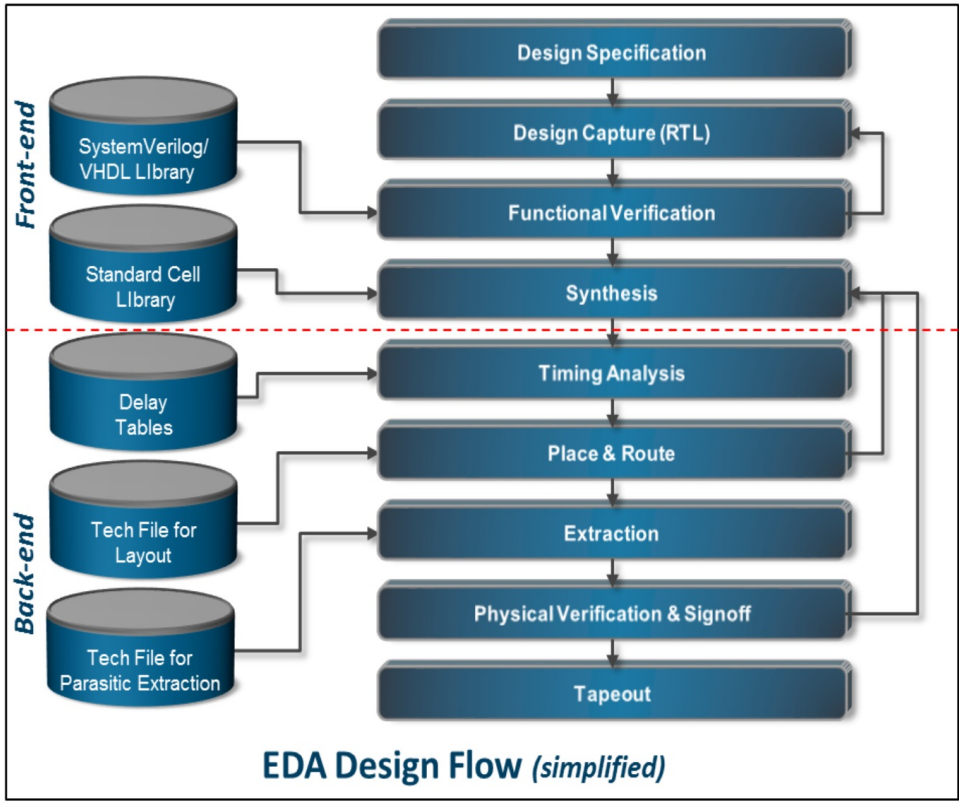
1982-1985

Digitalization begun

Thriller (1982), Epic Records. Cover photo by Dick Zimmerman

1980s was also the Decade of Automated Design

The basic scheme of automated design was set then



- Fully synchronous design
  - Verilog and VHDL
  - Logic simulation and synthesis
  - Scan-based test
  - Timing analysis and assurance
- >2 Layers of Metal
  - Over-the-cell routing
  - LEF, DEF, ECO…
- Design rule checking
  - Basis for mask rule checking later
- Workstations and ISVs with TBLs*

* Independent software vendors with term-based licenses

We Were Computationally Limited Back Then

IBM 3090: 30 MIPS, 50 MFLOPS, 126GB disk, 128MB RAM, 100KWatts, $20M

Source: Cray

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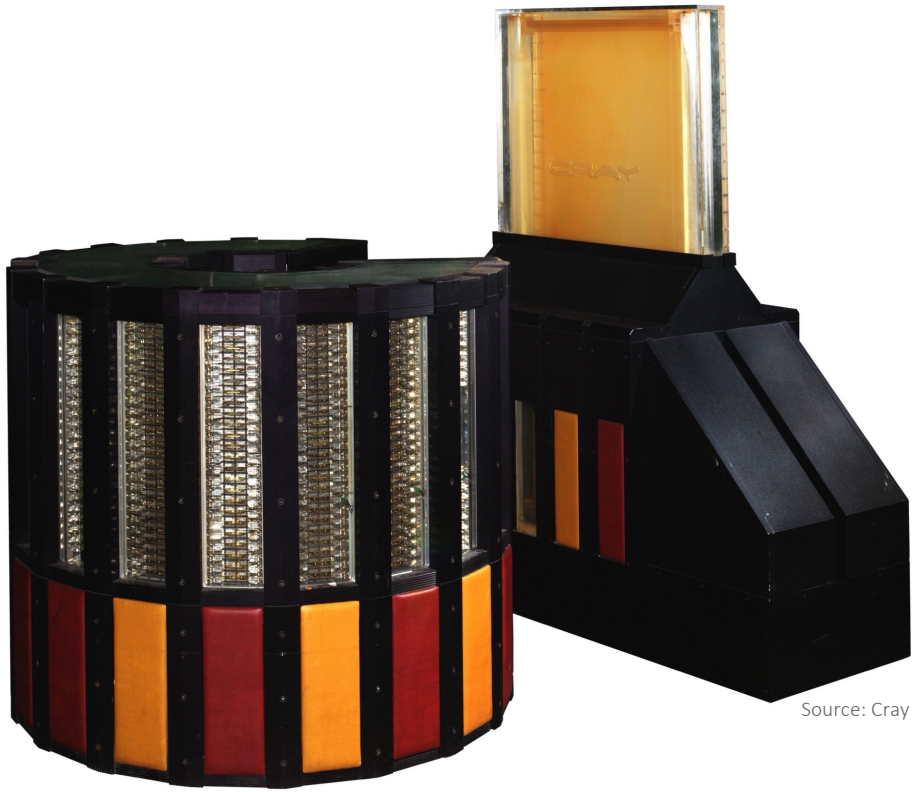
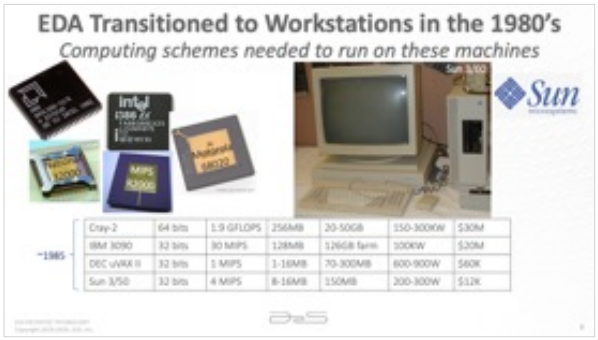


Source: Cray

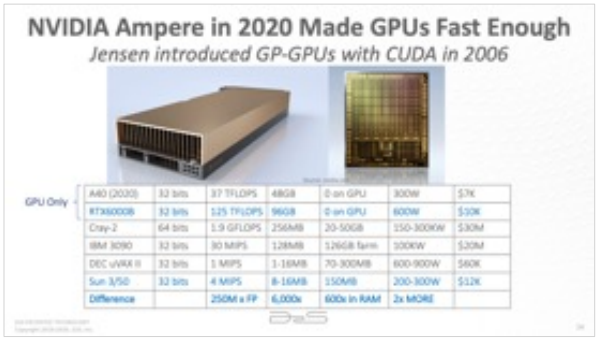
Source: IBM

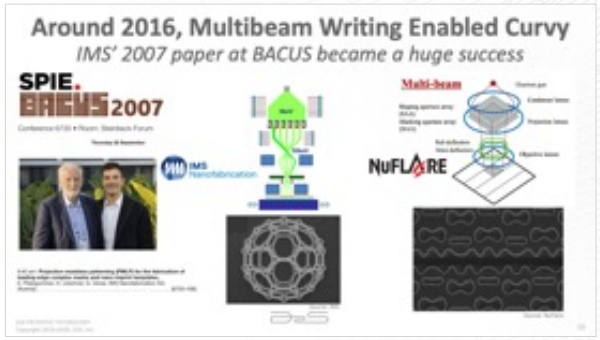
History is Repeating Itself

1975-1985 : Manhattan



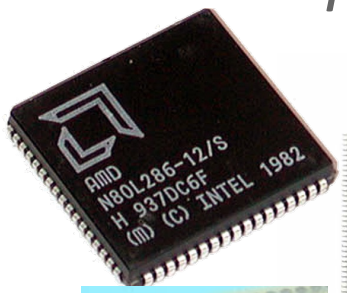
2007-2020 : Curvy





EDA Transitioned to Workstations in the 1980's

Computing schemes needed to run on these machines



Sun microsystems

~1985

Cray-2	64 bits	1.9 GFLOPS	256MB	20-50GB	150-300KW	$30M
IBM 3090	32 bits	30 MIPS	128MB	126GB farm	100KW	$20M
DEC uVAX II	32 bits	1 MIPS	1-16MB	70-300MB	600-900W	$60K
Sun 3/50	32 bits	4 MIPS	8-16MB	150MB	200-300W	$12K

EDA Transitioned to Workstations in the 1980's

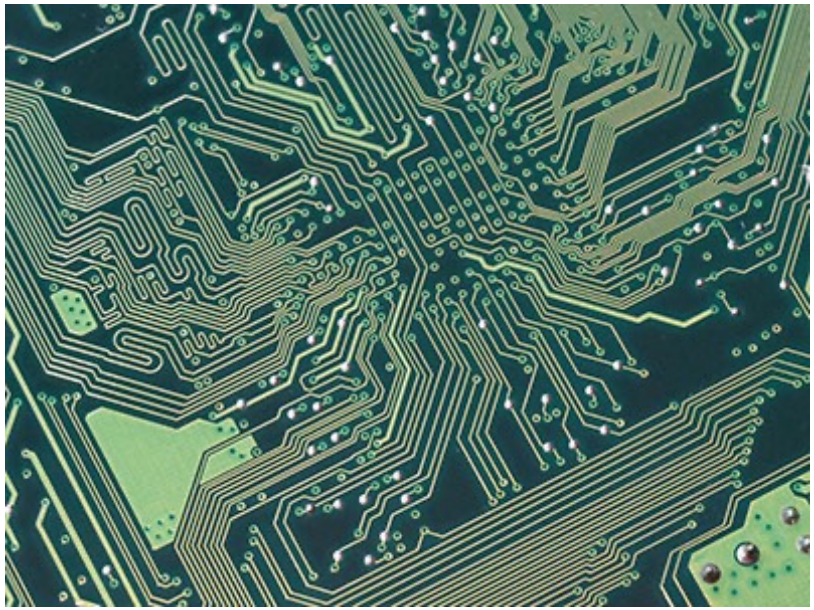
We had to design to machines 4000x less than Apple Watch

Sun microsystems

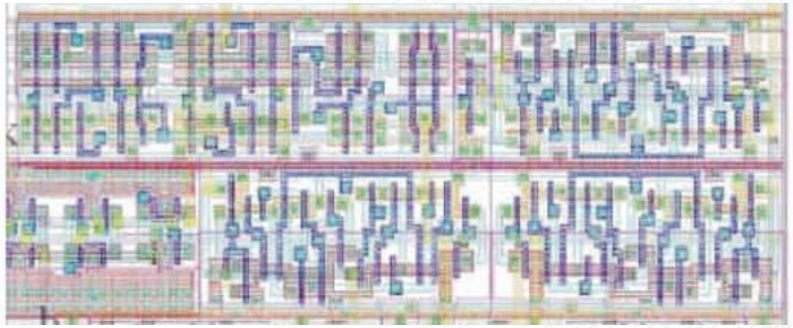
~1985	Cray-2	64 bits	1.9 GFLOPS	256MB	20-50GB	150-300KW	$30M
	IBM 3090	32 bits	30 MIPS	128MB	126GB farm	100KW	$20M
	DEC uVAX II	32 bits	1 MIPS	1-16MB	70-300MB	600-900W	$60K
	Sun 3/50	32 bits	4 MIPS	8-16MB	150MB	200-300W	$12K
	Apple Watch	64 bits	2 GFLOPS	1GB	64GB	1-2W	$400

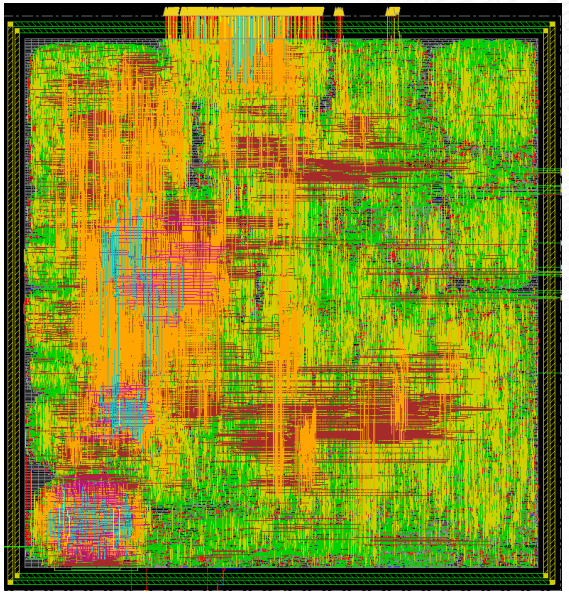
Computing Limited Chip Routing to Manhattan

Needed to break away from PCB-based routing schemes



Source: ourpcb.com





Source: Vladimir Stojanovic, course materials for 6.973 Communication System Design, Spring 2006. MIT OpenCourseWare

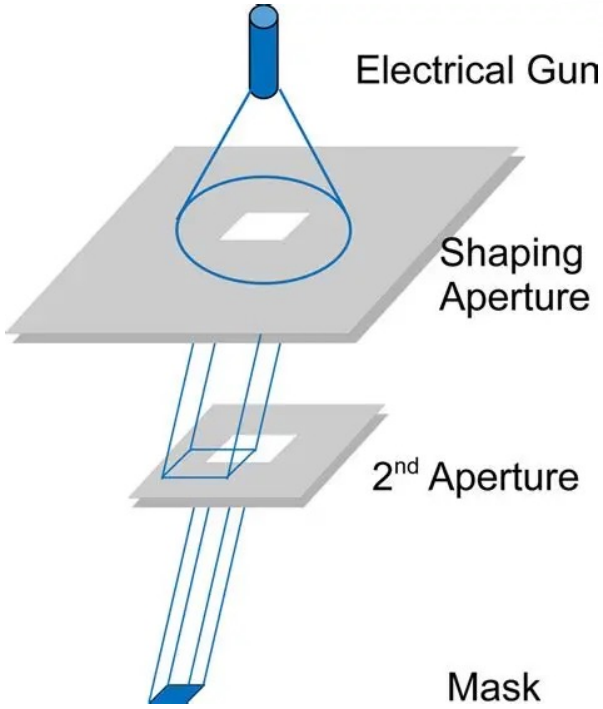
Source: University of Bremen

At the Same Time, Mask Writing Went Manhattan, too

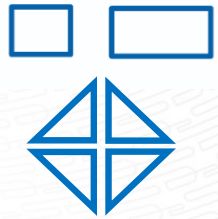
4X masks and commercial VSB writers arrived about 1985

H. C. Pfeiffer

IBM

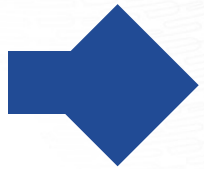


Source: University of Texas, Austin



VSB Basic Primitives

JEOL



NuFlare's 2nd Aperture

NUFLARE

D2S

Around 2016, Multibeam Writing Enabled Curvy

IMS' 2007 paper at BACUS became a huge success

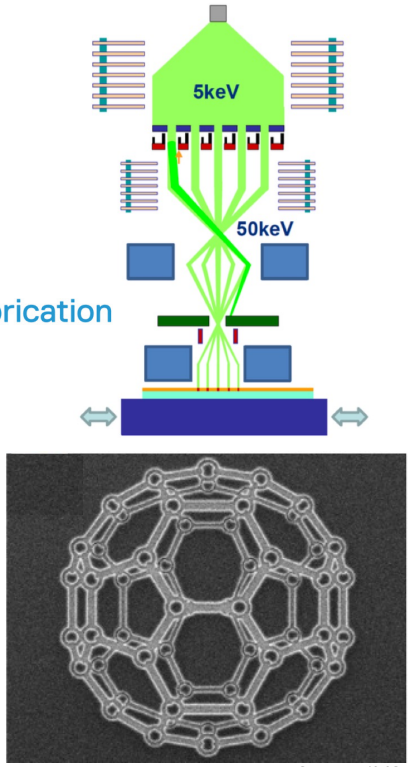
SPIE. BACUS 2007

Conference 6730 • Room: Steinbeck Forum

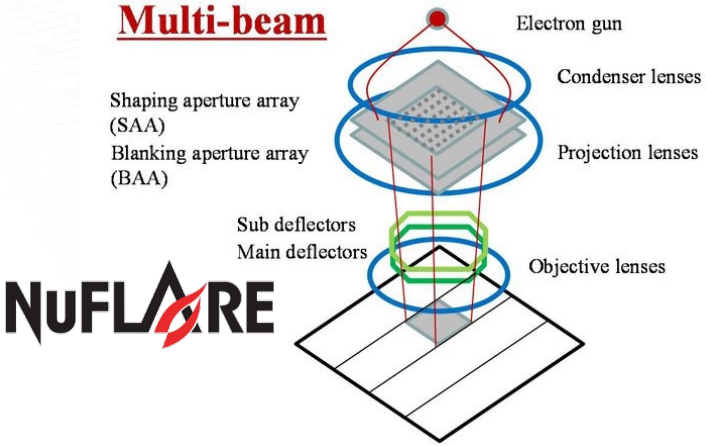
Thursday 20 September

IMS Nanofabrication

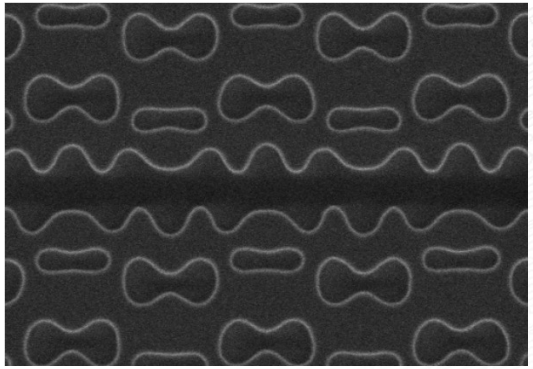
9:40 am: **Projection maskless patterning (PMLP) for the fabrication of leading-edge complex masks and nano-imprint templates,**
E. Platzgummer, H. Löschner, G. Gross, IMS Nanofabrication AG (Austria) . . . . . [6730-108]



Source: IMS



NuFlare

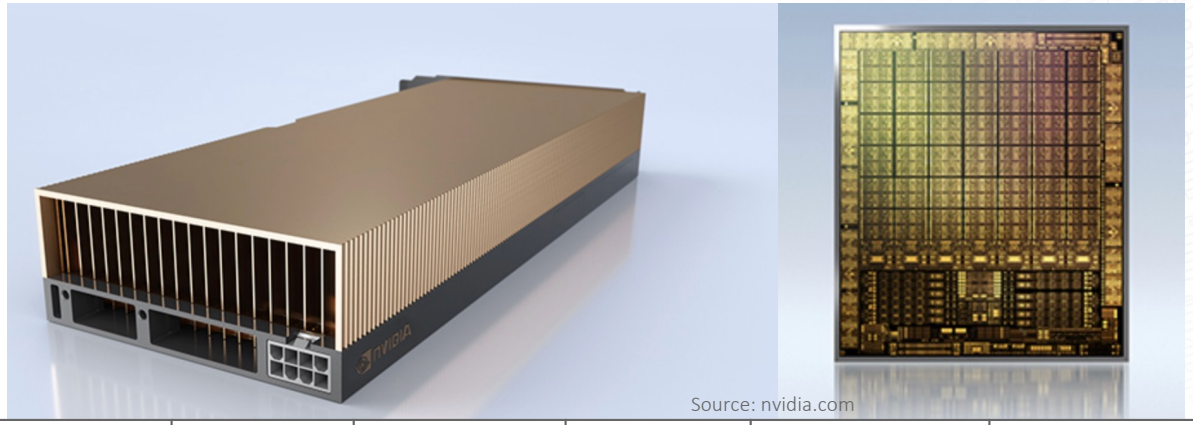


Source: NuFlare

D2S

NVIDIA Ampere in 2020 Made GPUs Fast Enough

Jensen introduced GP-GPUs with CUDA in 2006



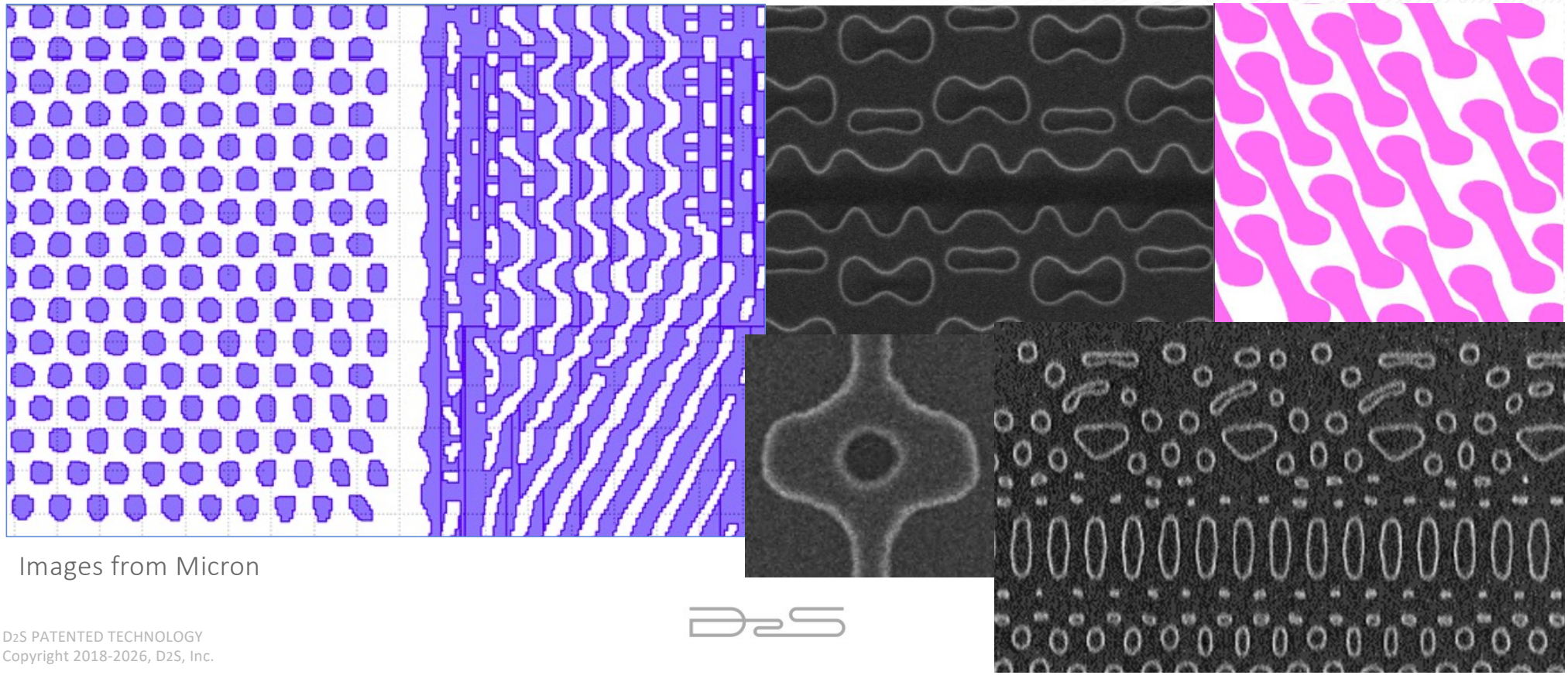
Source: nvidia.com

GPU Only

A40 (2020)	32 bits	37 TFLOPS	48GB	0 on GPU	300W	$7K
RTX6000B	32 bits	125 TFLOPS	96GB	0 on GPU	600W	$10K
Cray-2	64 bits	1.9 GFLOPS	256MB	20-50GB	150-300KW	$30M
IBM 3090	32 bits	30 MIPS	128MB	126GB farm	100KW	$20M
DEC uVAX II	32 bits	1 MIPS	1-16MB	70-300MB	600-900W	$60K
Sun 3/50	32 bits	4 MIPS	8-16MB	150MB	200-300W	$12K
Difference		**250M x FP**	**6,000x**	**600x in RAM**	**2x MORE**	

Now That Computing Isn't Limited

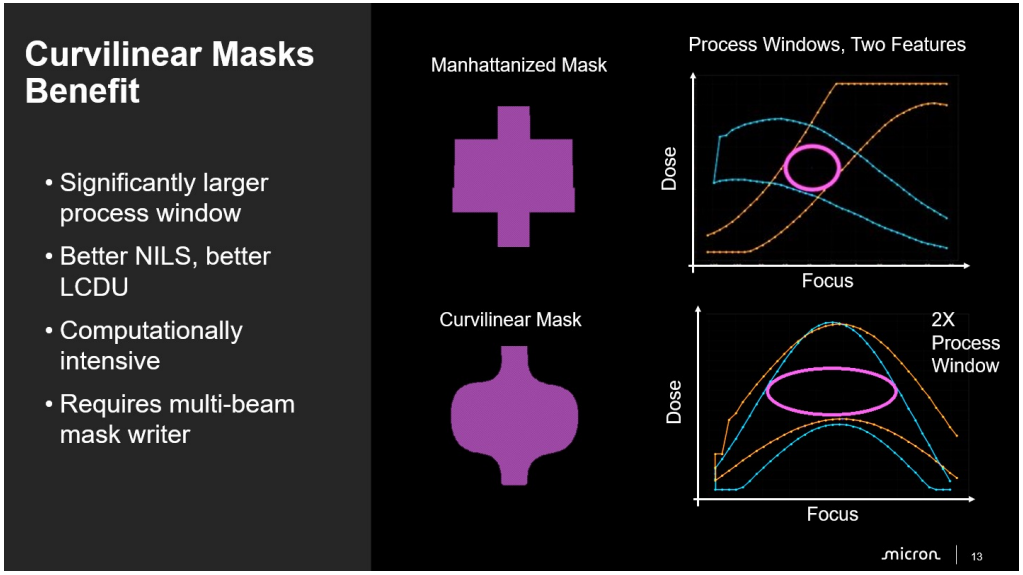
Entirely curvilinear masks are inevitable



Images from Micron

Only Entirely Curvilinear Masks are Manufacturable

But not all curvy masks are entirely manufacturable masks



Source: Micron

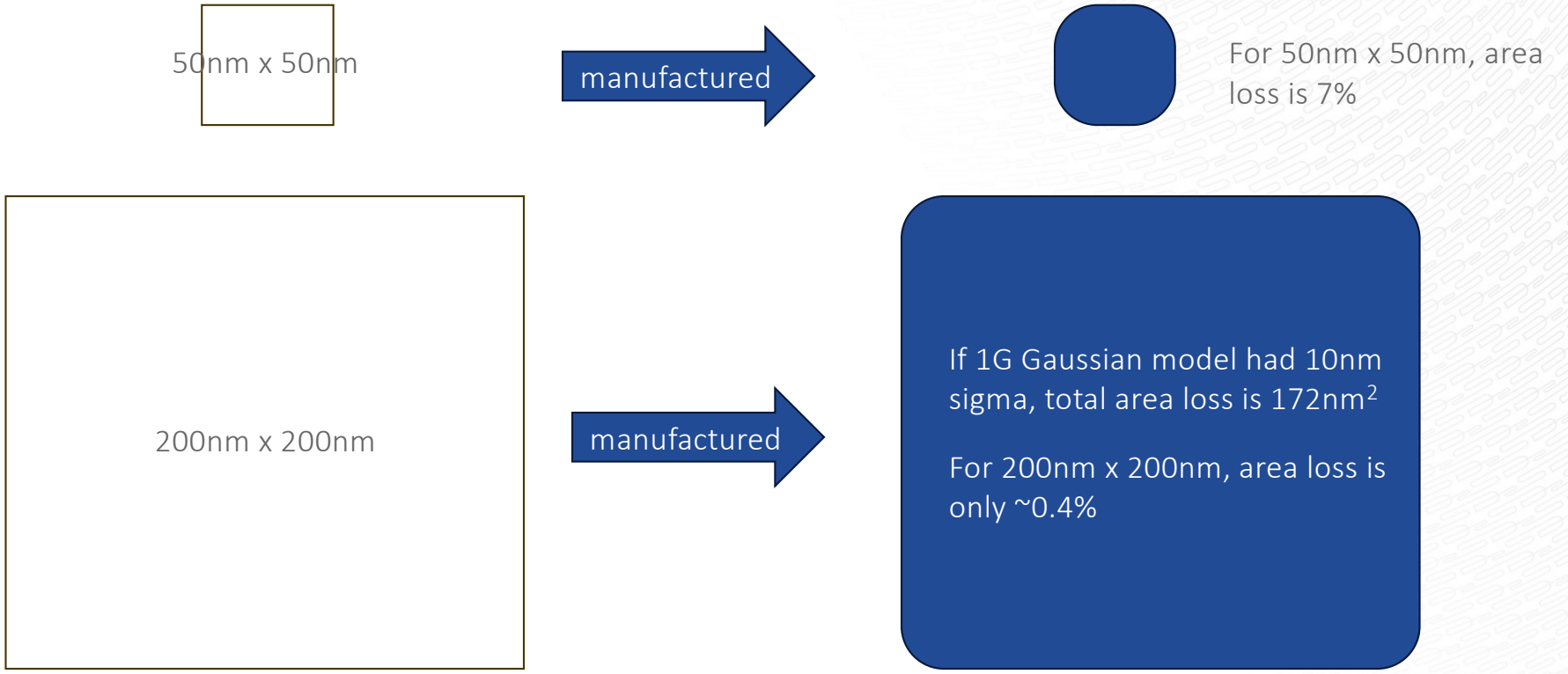
Four reasons for curvy masks

1. 2X Process Window
2. Manufacturable masks:
   Ask for what you can get, and get what you asked for
3. Manufacturable masks:
   Best area uniformity on mask for best wafer CDU
4. Enables curvy designs

Wafer Accuracy is About Area Accuracy on Mask

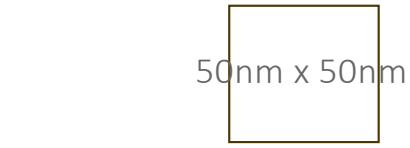
So smaller shapes we need to handle now can't be doing 1D on mask

This is already true for all decorated OPC masks before Curvy…



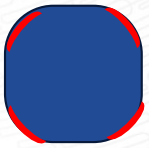
Unmanufacturable Shapes Always Have Bad Dose Margin

Instance-to-instance mask area uniformity is critical for wafer CDU



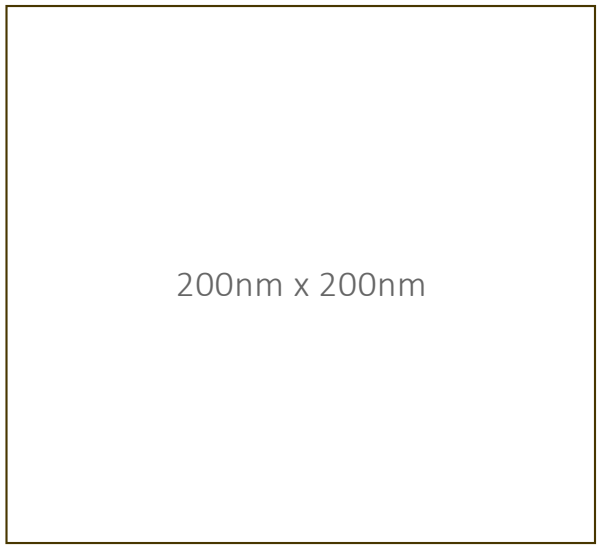
manufactured

Poor dose margin on corners

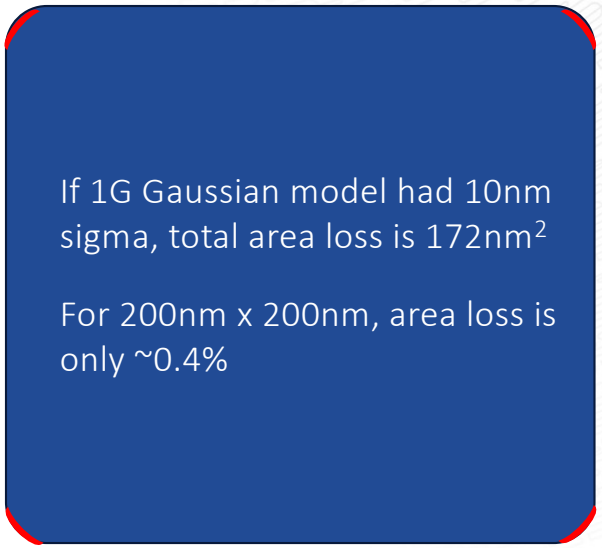


For 50nm x 50nm, area loss is ~~7~~%

6-8% depending on instance



manufactured



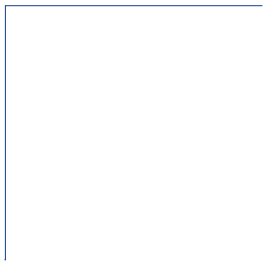
If 1G Gaussian model had 10nm sigma, total area loss is 172nm^2

For 200nm x 200nm, area loss is only ~0.4%

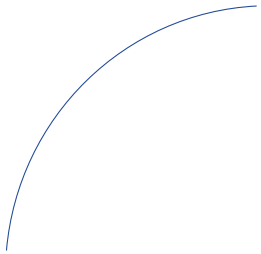
Much Better to Ask for What You Can Get

Instance-to-instance variation is critical for manufacturing

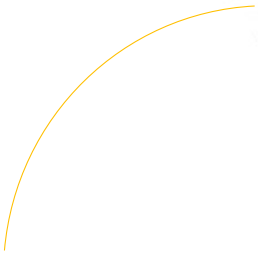
Trying to manufacture this



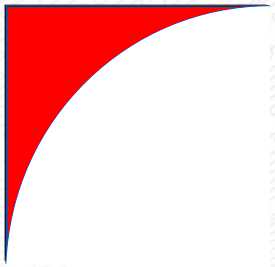
and getting this



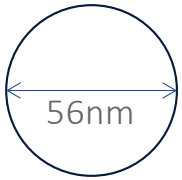
has more variation than trying to manufacture this



because the dose of this area changing +/-x% makes a big difference.

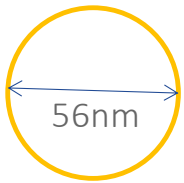


If you ask for what you can get…



manufactured

You get better mask area uniformity and therefore, better wafer CDU



Ask for what you can get

And get what you asked for,

It will be manufactured as you litho simulated,

and with better mask area uniformity, and wafer CDU