A Memory Maker's Perspective on Advanced Lithography for DRAM Applications

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micron Intelligence Accelerated™

eBeam Initiative Luncheon
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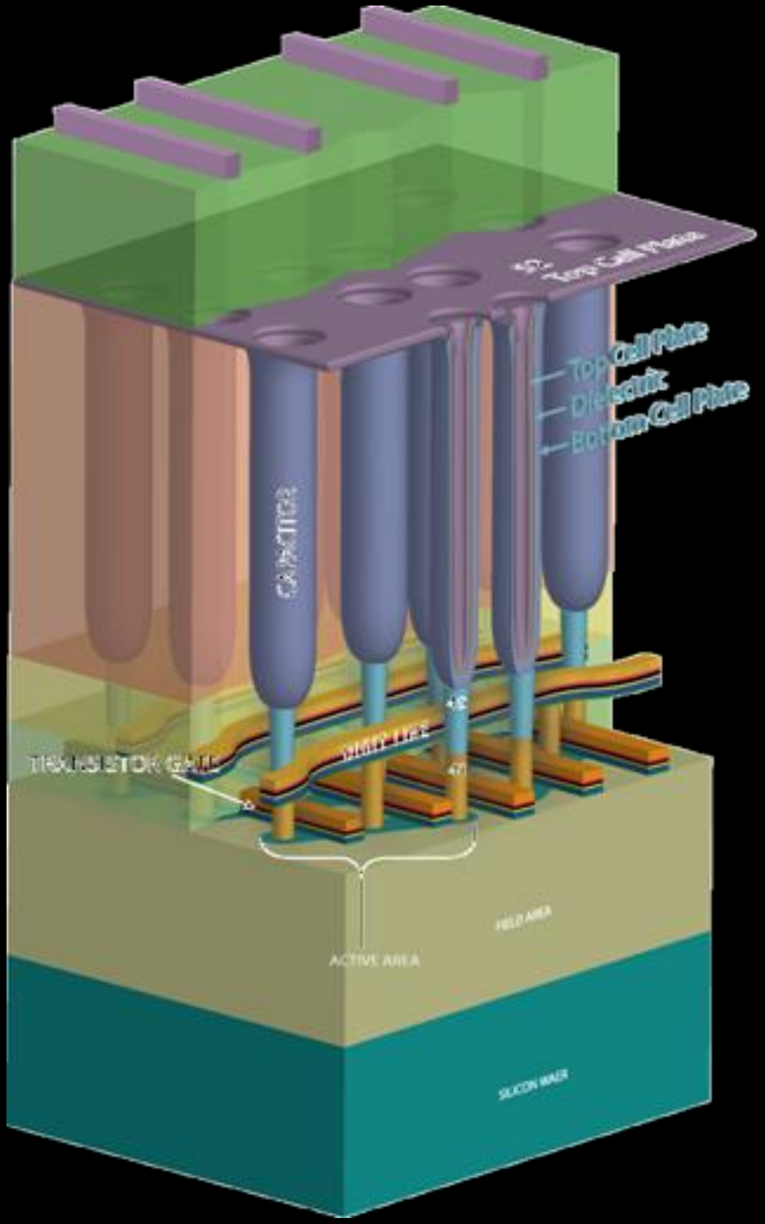
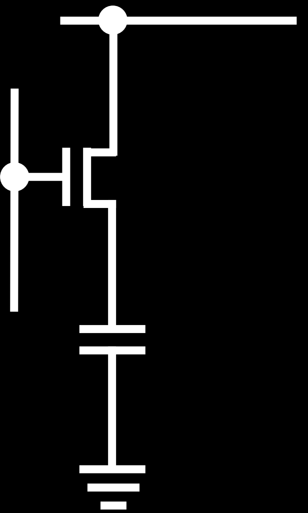
DRAM Memory

- Main memory for cell phones, laptops, and servers
- Fastest access times and lowest energy among all memory types
- High-performance graphics, supercomputing, autonomous driving and artificial intelligence all require high levels of DRAM memory

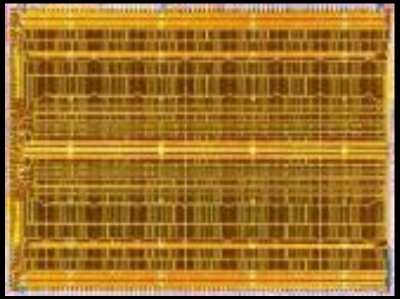


DRAM Memory Cell



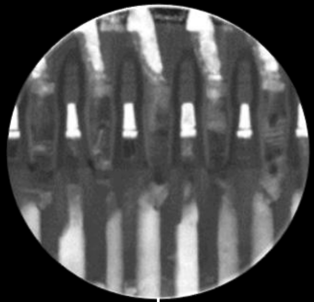
DRAM: 3 Nodes of Technology Leadership

Scaling for cost and performance improvement, and funding pathfinding activities to meet diverging requirements and product offerings



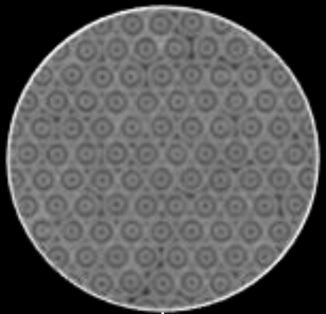
1β Mature Node in HVM

Advanced CMOS

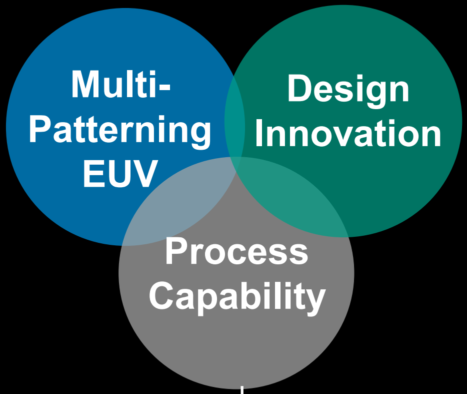


1γ HVM Production

EUV introduction



1δ Development



Multi-Patterning EUV

Design Innovation

Process Capability

1ε Pathfinding

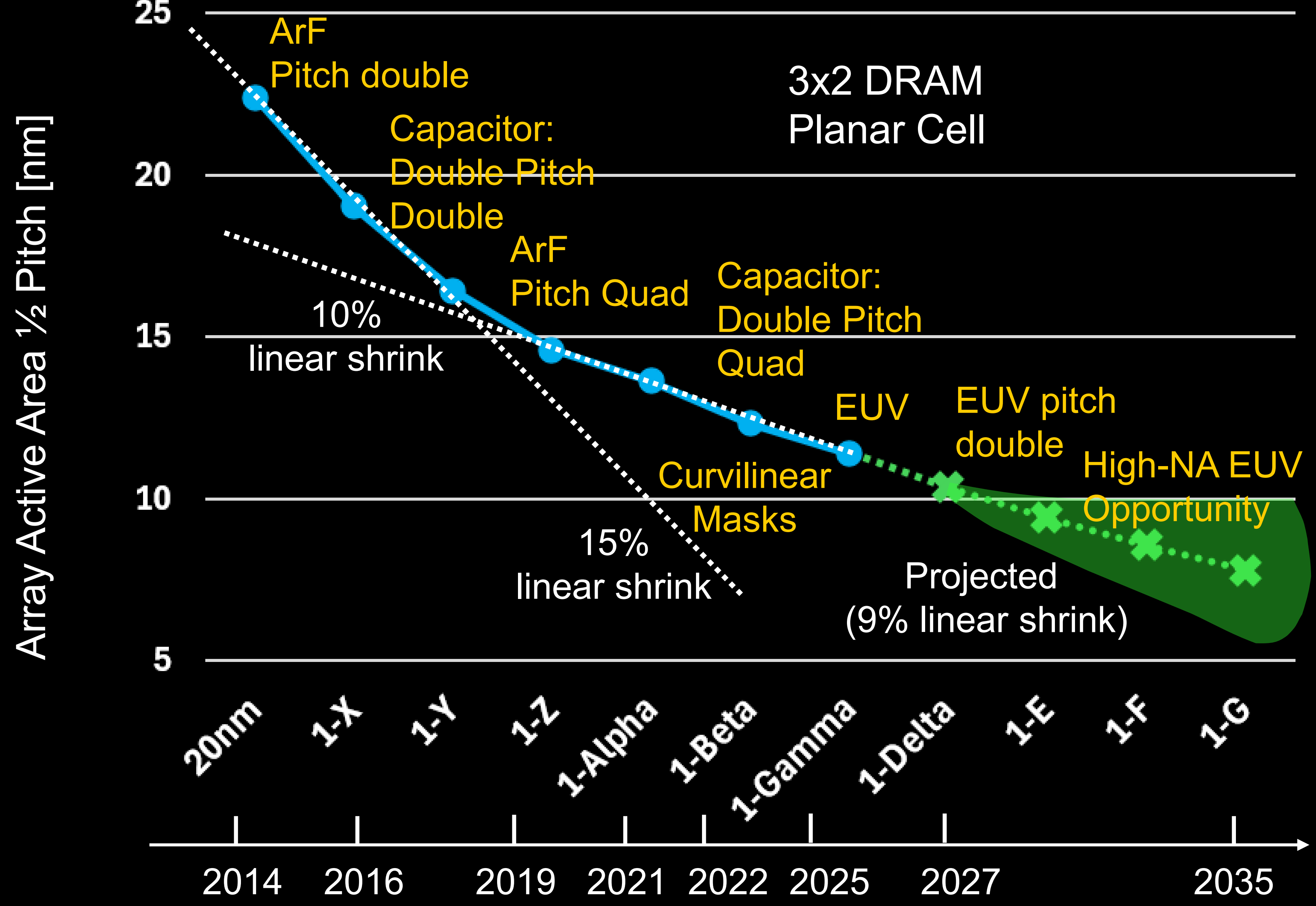
Extending planar DRAM roadmap
High-NA EUV R&D Investment

Development

Continued investment in 3D DRAM R&D

First to market with
1α, 1β, 1γ
next-generation process nodes

DRAM Scaling: Patterning Techniques for Critical Levels



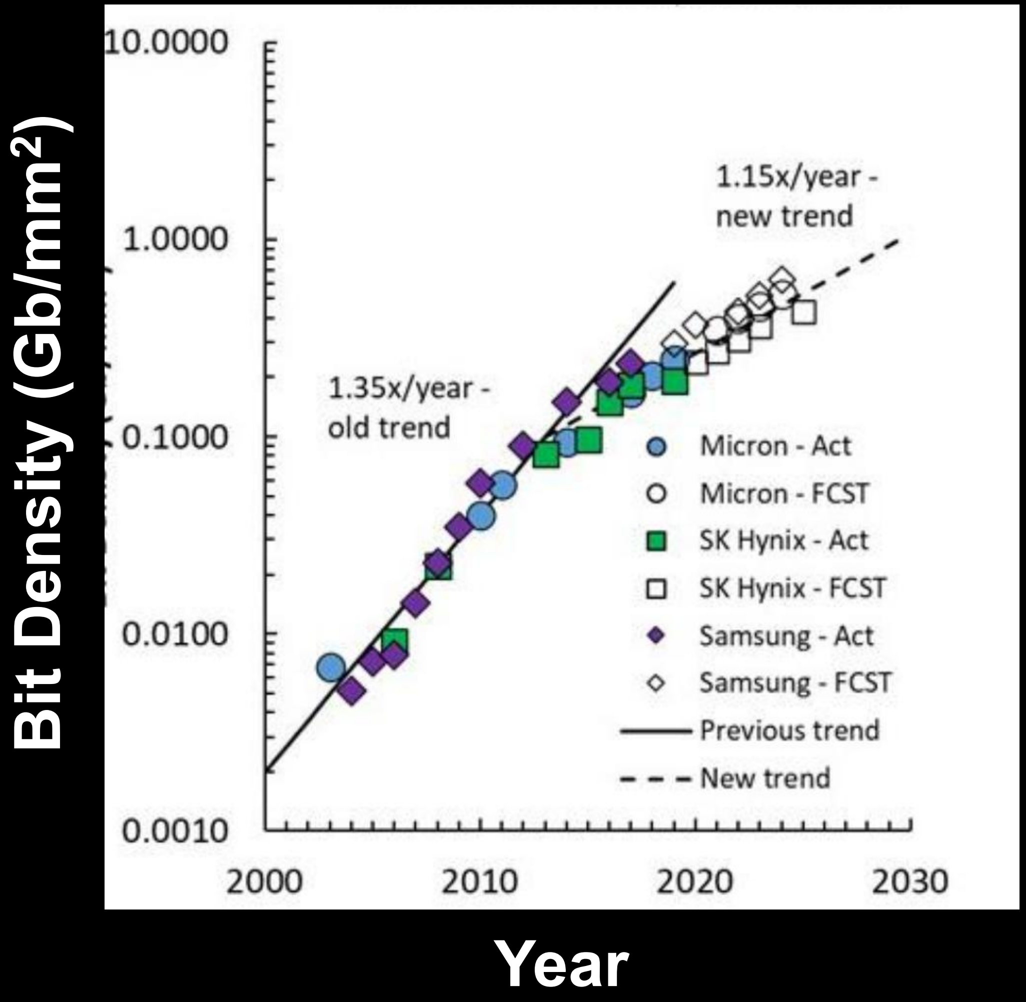
Future roadmap diverging:

- Planar DRAM
- 4F2 vertical
- 3D-DRAM

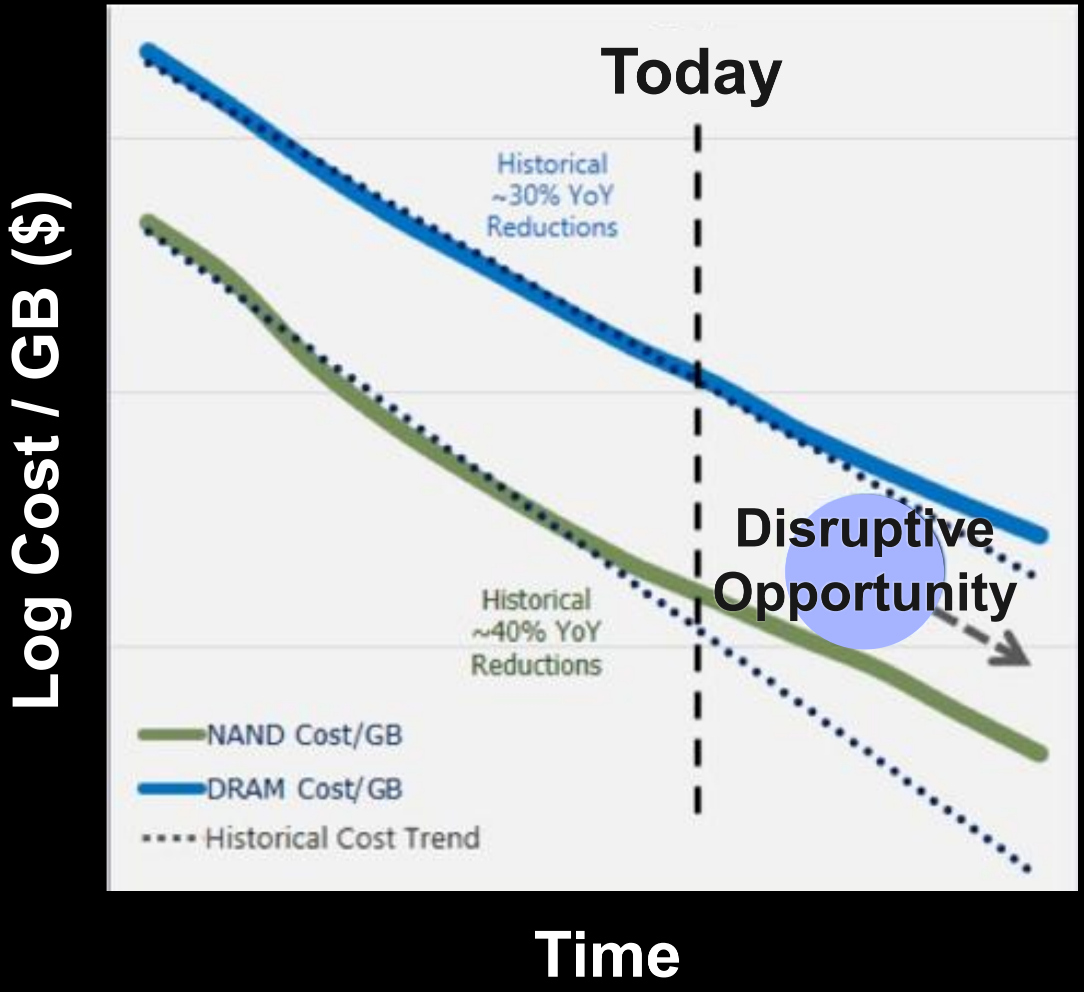
→ Different lithographic requirements

DRAM Moore’s Law and Opportunity for New Memory

DRAM Bit Density Over Time

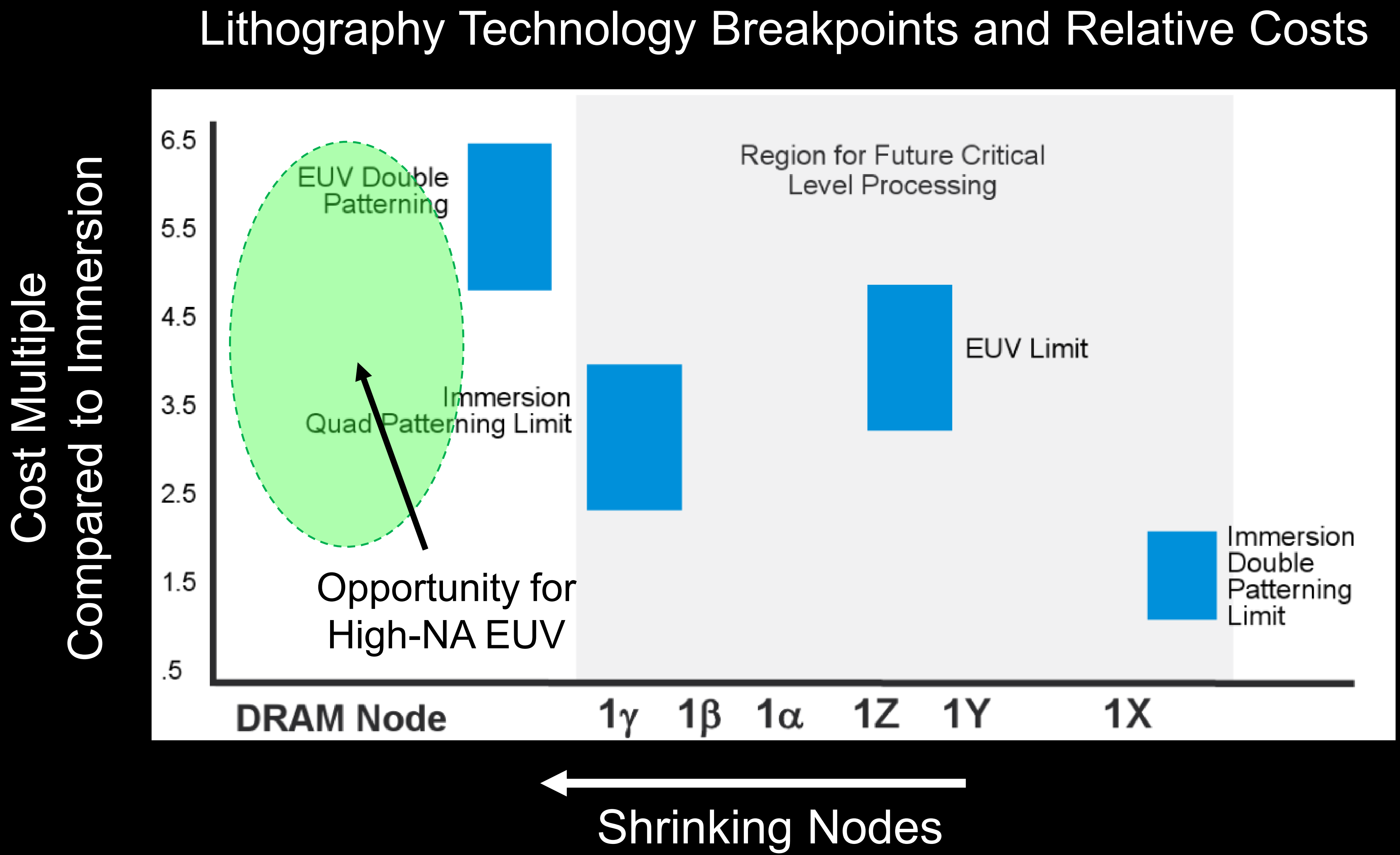


Cost Reduction Over Time



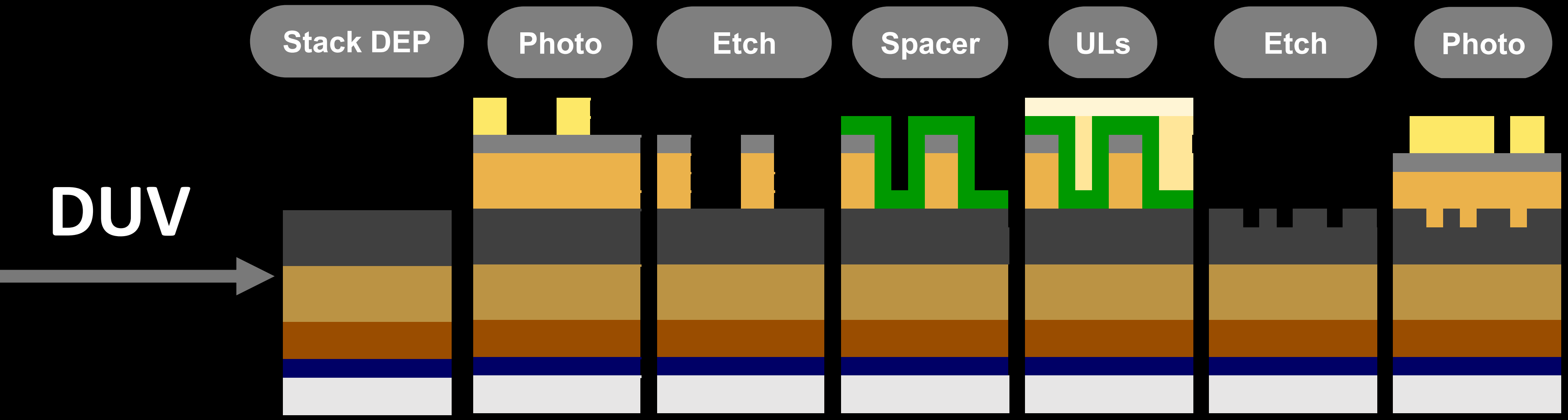
From Tech Insights:
https://semiwiki.com/semiconductor-services/297904-spie-2021-applied-materials-dram-scaling/

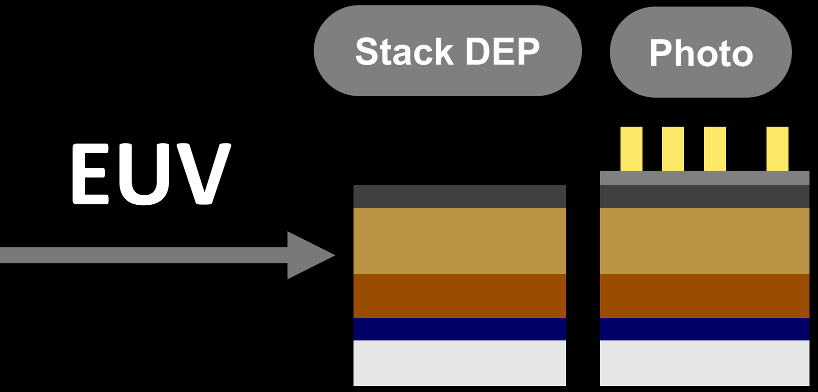
DRAM Lithography and Patterning Strategies

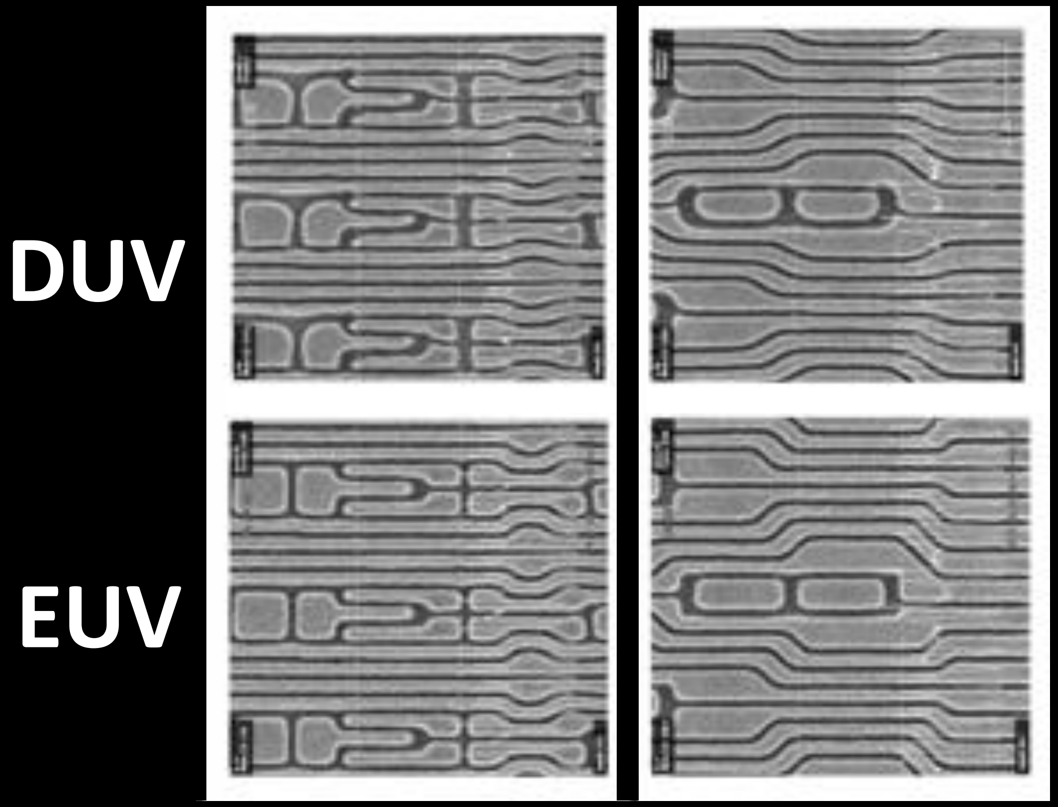


- Micron’s pattern multiplication is a strategic advantage

Why EUV?





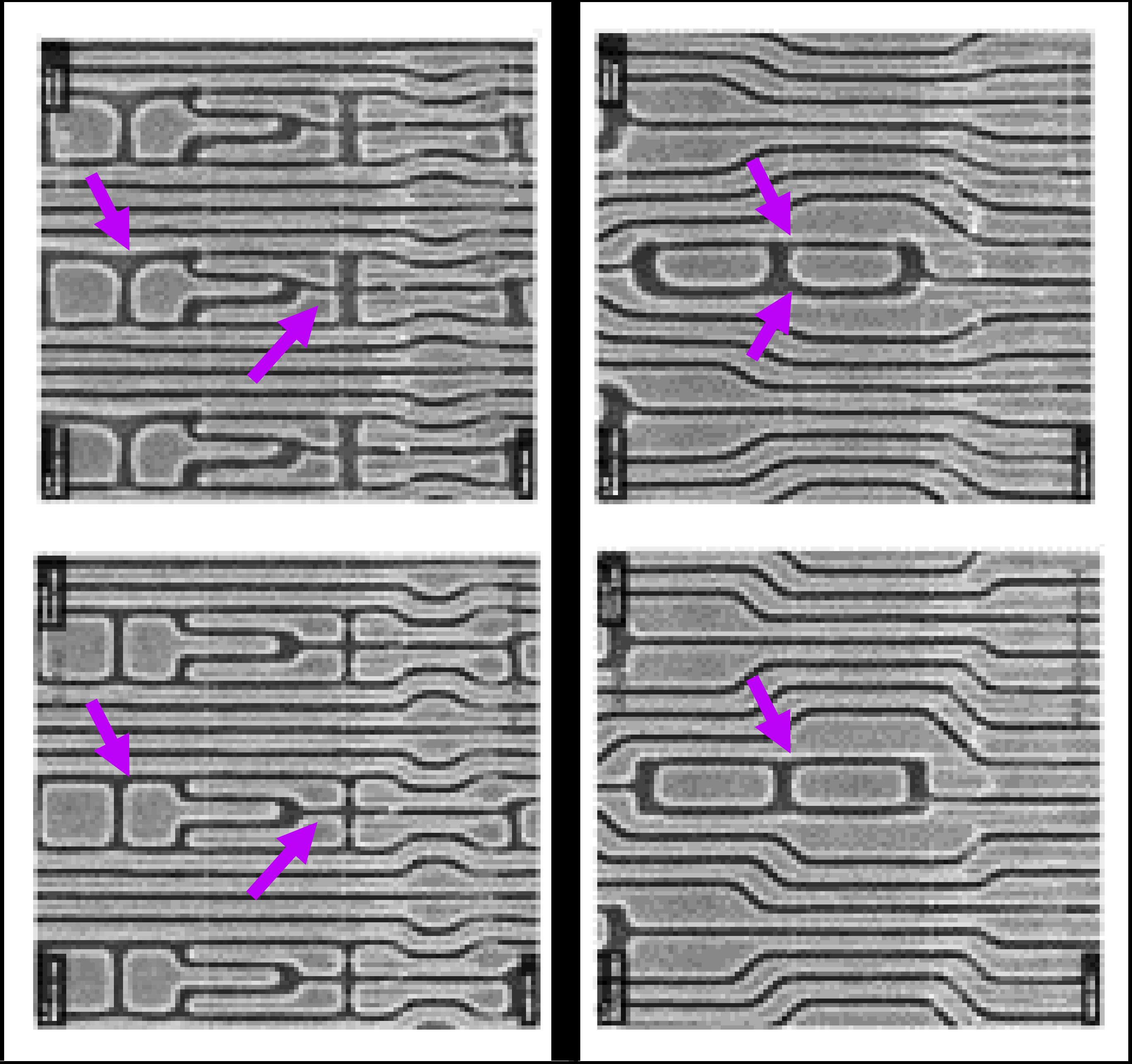


- Same pattern in significantly fewer steps
- Fewer design rule limitations

DRAM Metal0

DUV
Pitch-multiplied

EUV
Single patterning



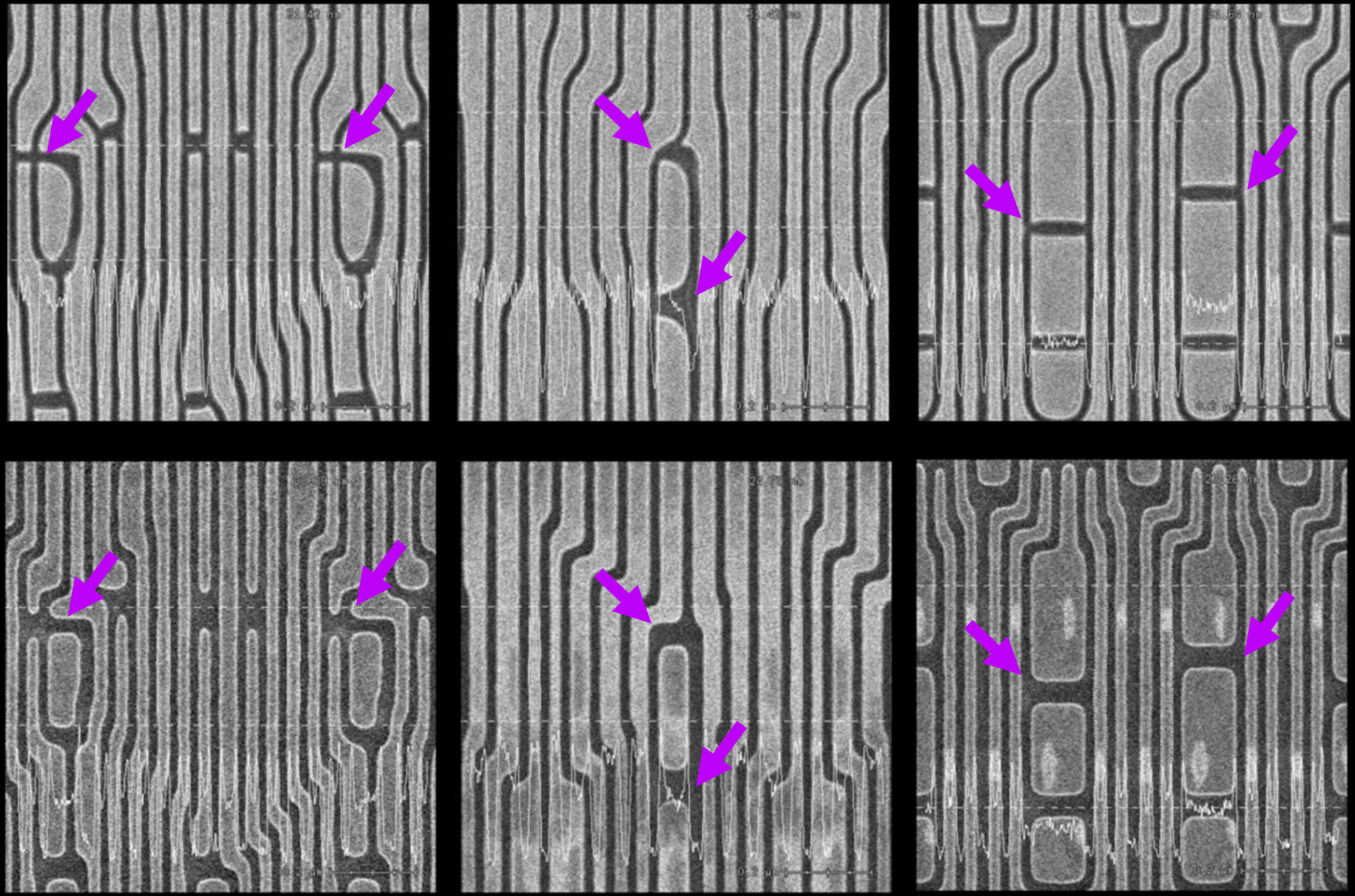
- Corners defined by lithography are rounded
- Larger pattern variability

- Improved corner rounding
- Improved pattern fidelity

DRAM Metal0 Layer Multi-Patterning vs. EUV Single Patterning

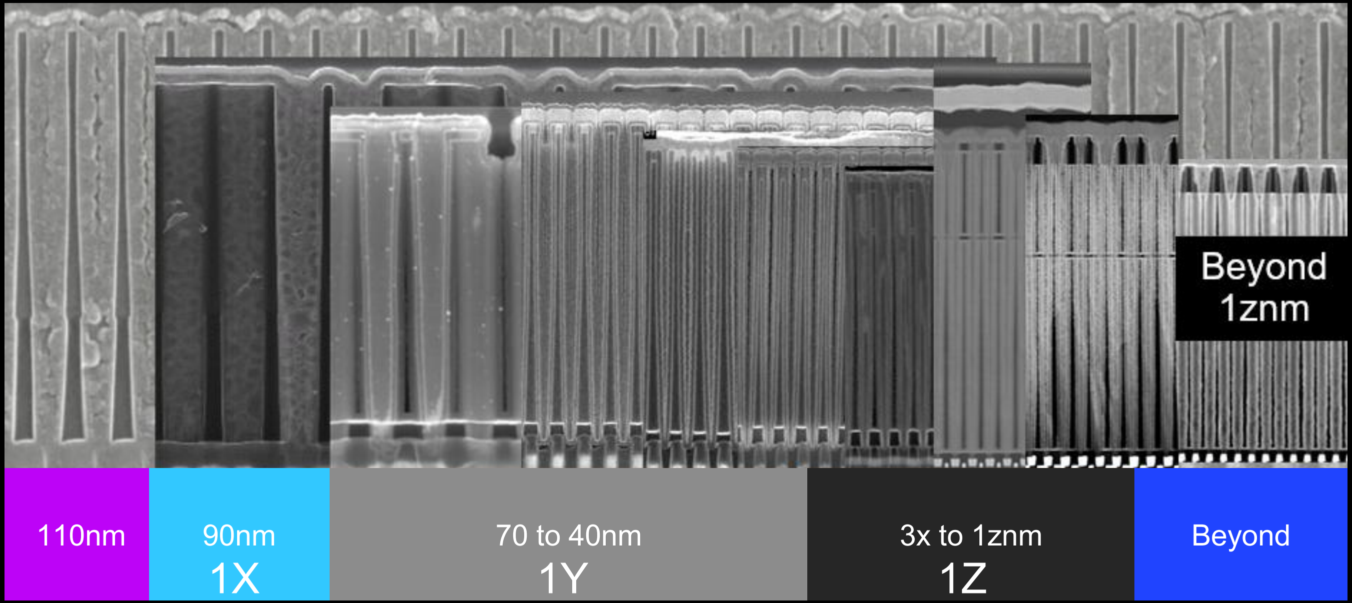
DUV
Pitch-multiplied

EUV
Single patterning



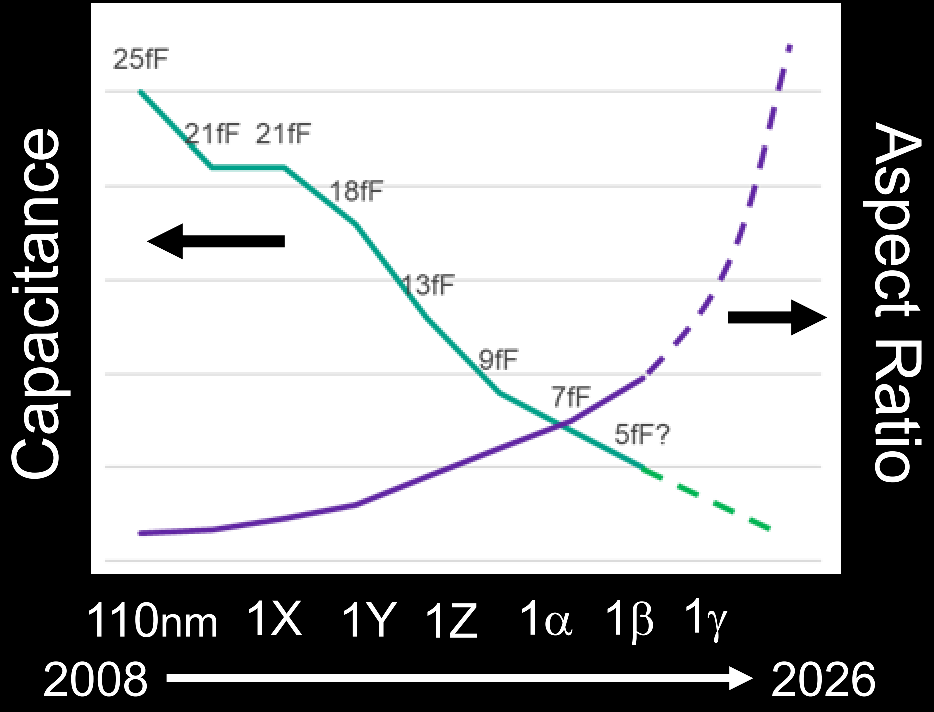
Scaling Challenges

Advanced technology nodes face increasingly complex and disruptive scaling challenges



Advanced patterning: EUV, multi-patterning
Structural and material innovations required to meet performance and power requirements

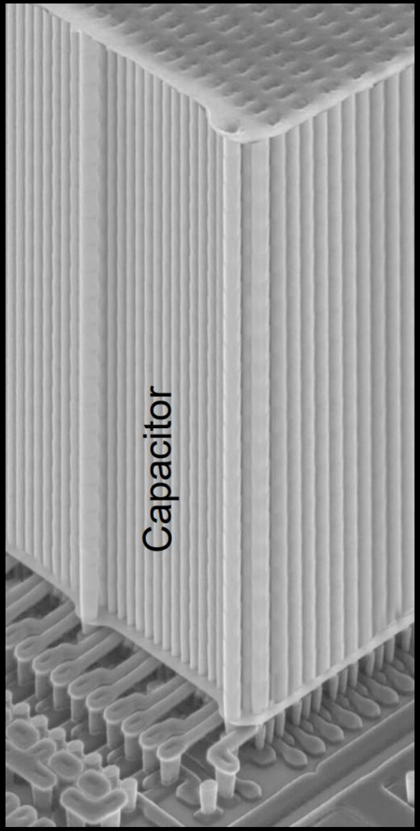
Capacitor Scaling



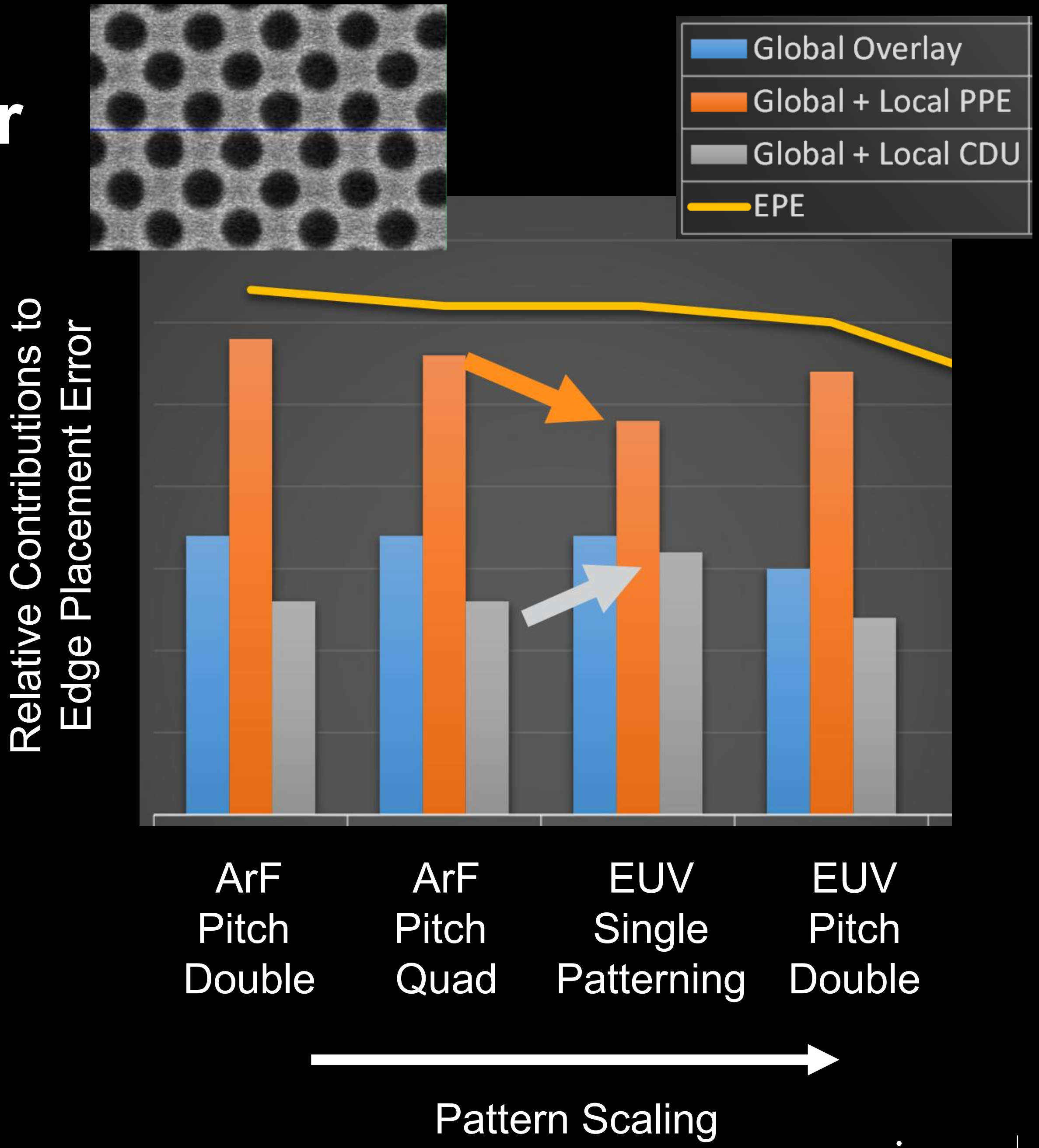
Further scaling may require disruptive innovation

Capacitor Aspect Ratio and Pattern Placement Error

Burj Khalifa
AR: ~5:1



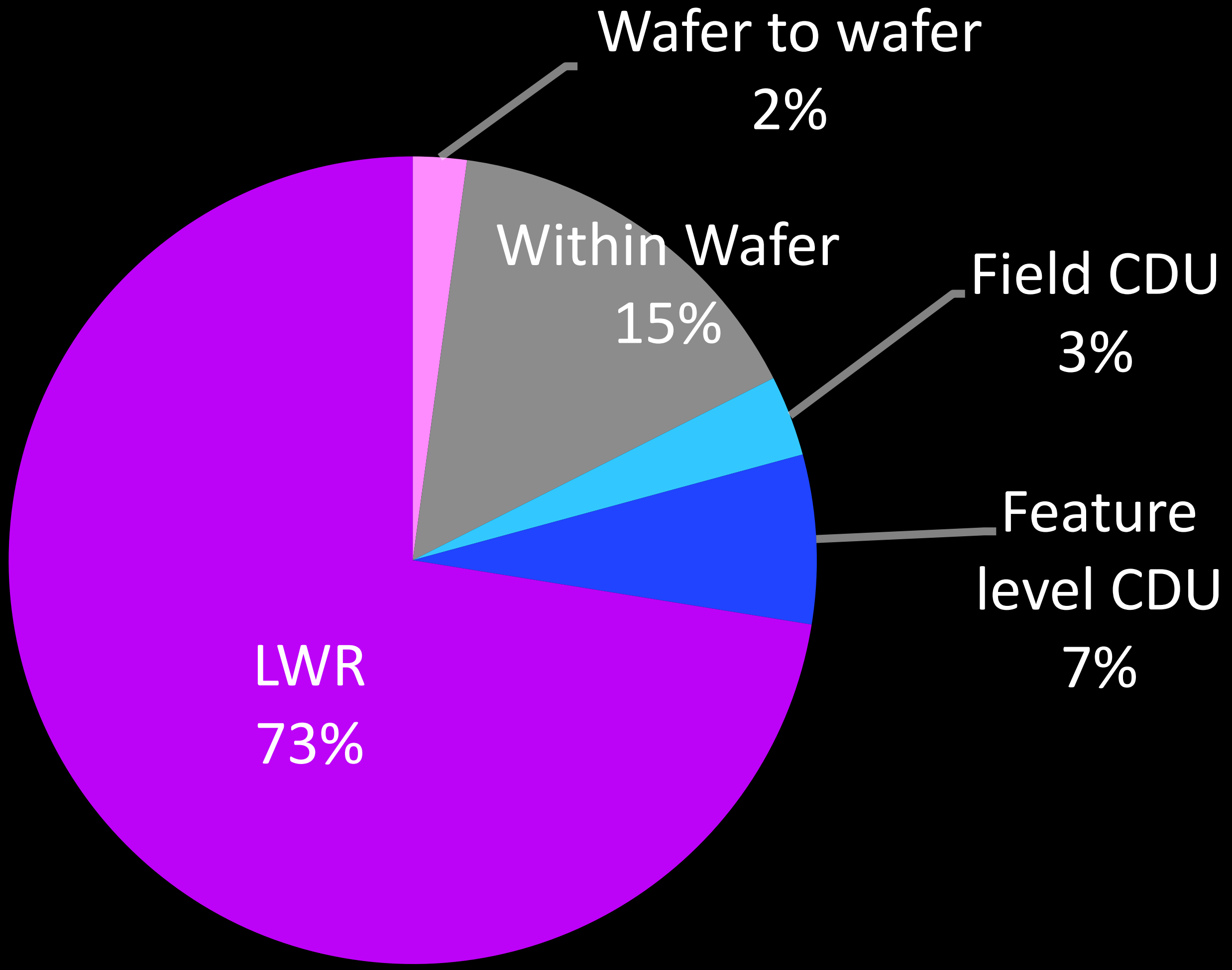
DRAM Capacitor
AR: 40:1 to 60:1



EUV Contributors to CD Uniformity

- EUV Stochastics
- Local CD variation (LCDU)
- Line Width Roughness (LWR)
- Edge Placement Error (EPE)
- Systematic variations: Wafer and Field signatures

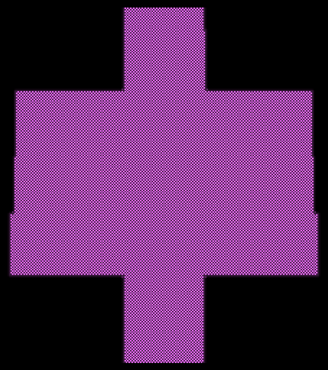
Dense Line Variation



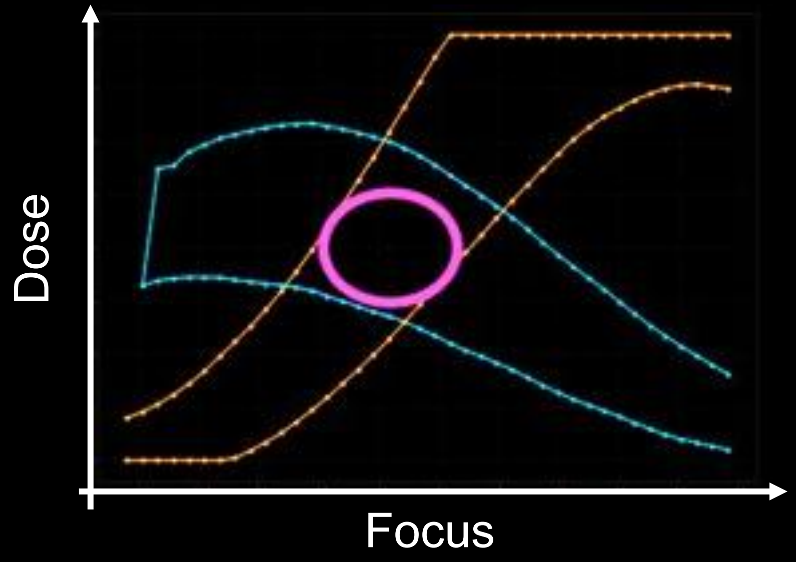
Curvilinear Masks Benefit

- Significantly larger process window
- Better NILS, better LCDU
- Computationally intensive
- Requires multi-beam mask writer

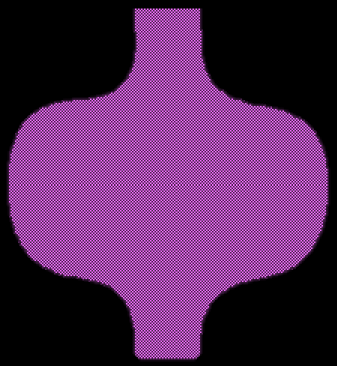
Manhattanized Mask

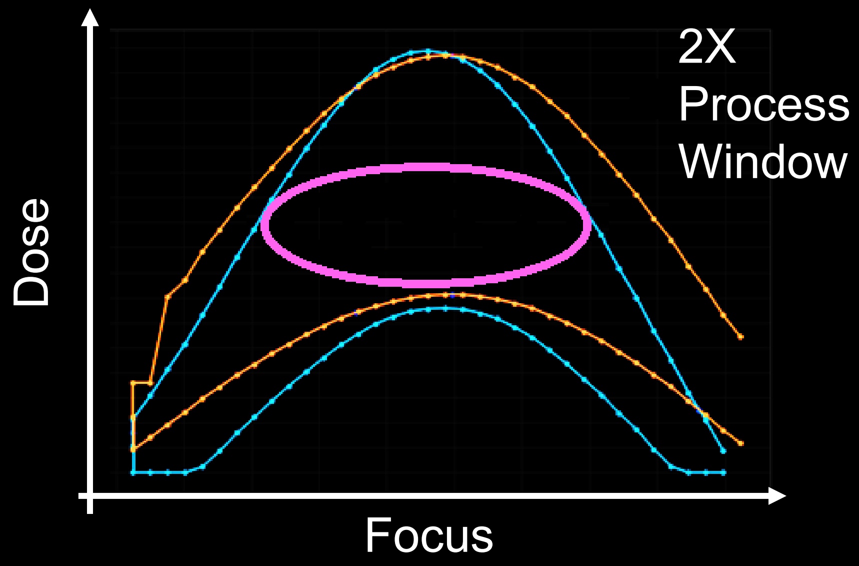


Process Windows, Two Features



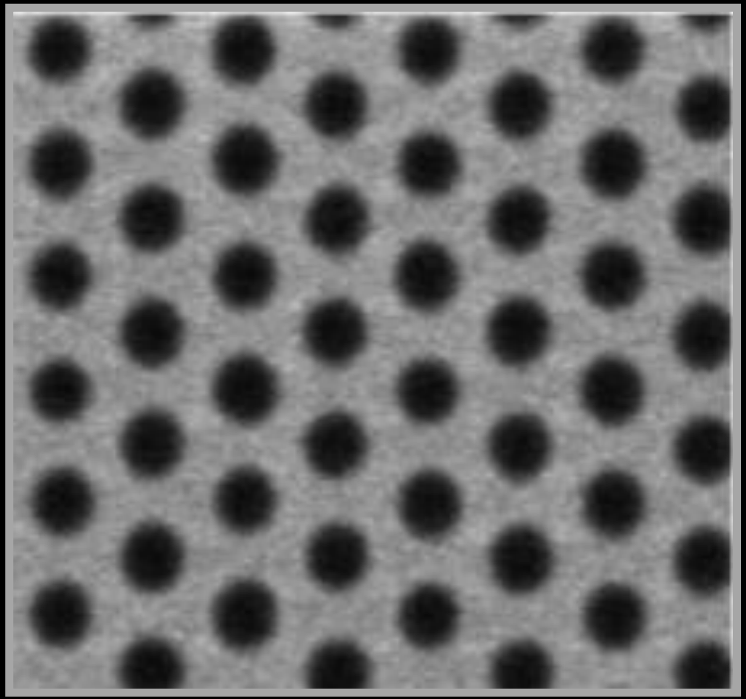
Curvilinear Mask



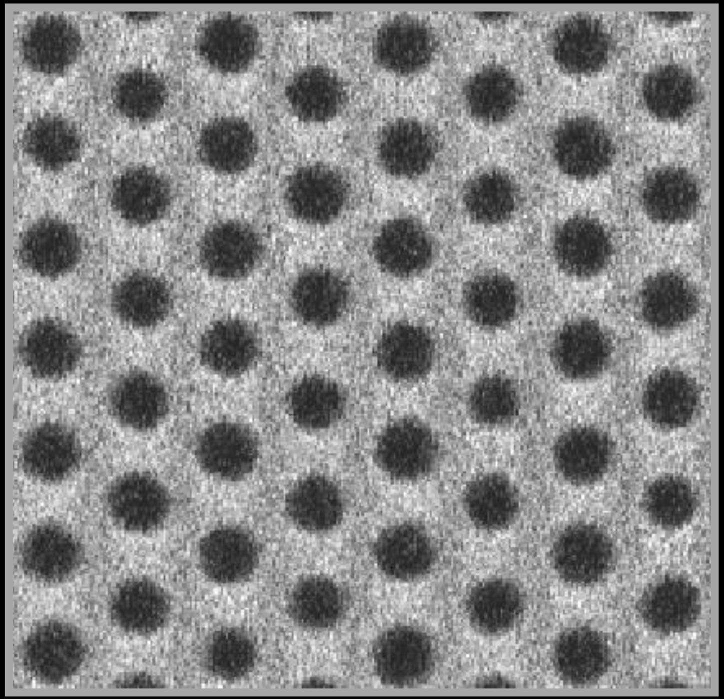


DRAM Array Hex Pattern: Capacitor and Pillar Pad

High-NA EUV Process Simplification



DUV Double Pitch Quad
~100 steps



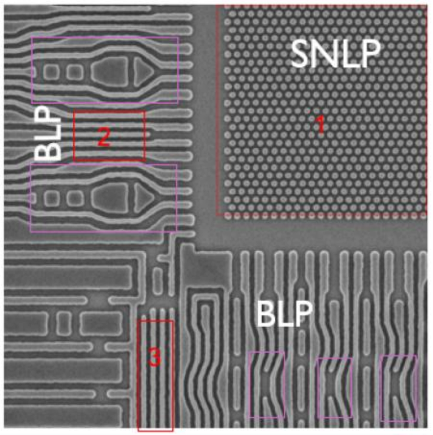
High-NA EUV
< 10 steps

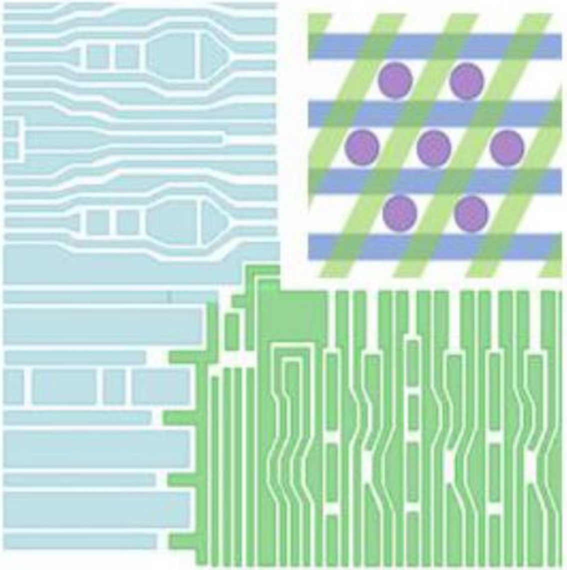
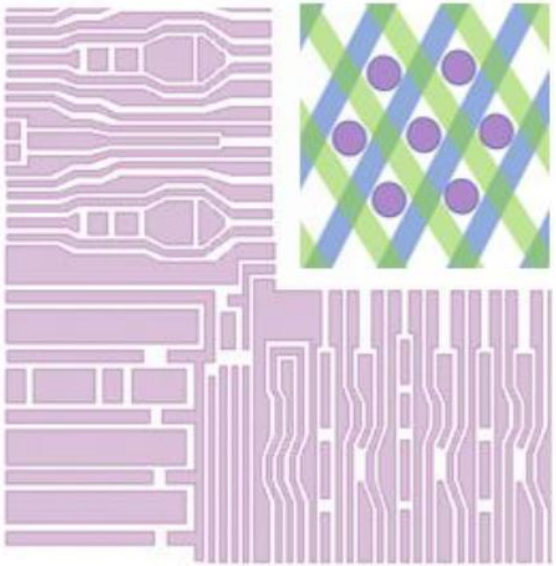
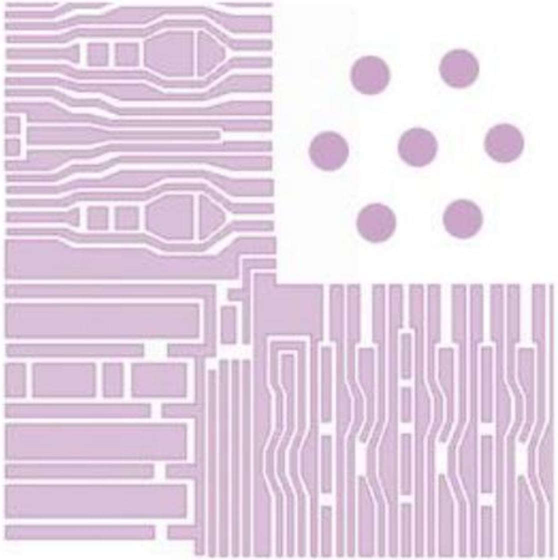
- CD Uniformity
- Pattern placement error
- Opportunity to combine several mask layers into one

Early exposure in ASML High-NA Lab

High-NA EUV Opportunity in DRAM

Following on the Steps of 0.33NA EUV:
Process and Mask Simplification

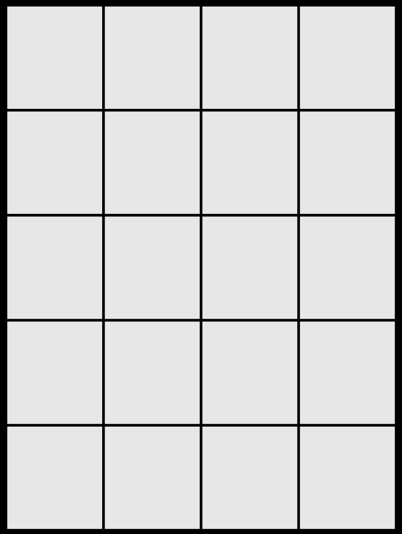


Solutions	Double Patterning Tech	Cross Multiple Patterning Tech	Single Patterning Tech
Design			

Patterning optimization for single mask bit-line-periphery and storage-node landing-pad DRAM layers using 0.33NA EUV lithography at the resolution limit
Van Tuong Pham, et al. (IMEC, KLA, Inpria)
Proc. of SPIE Vol. 12957 129570V-1 (2024)

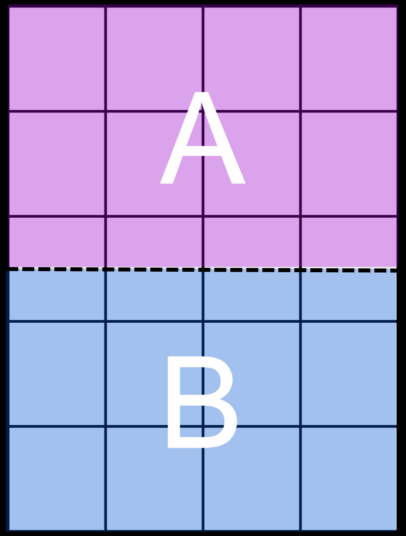
High-NA EUV
½ Field Exposure | Odd Die in Y

DUV, Low-NA EUV



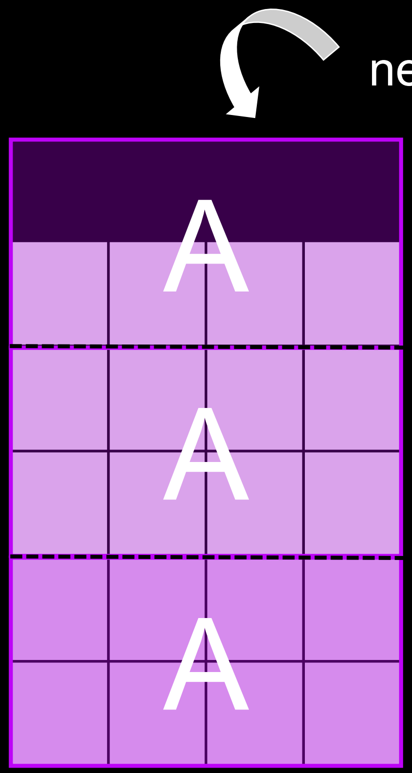
- Standard Field, 26mm x 33mm
- 5 die in Y

High-NA



- ~39% throughput loss (A/B reticle swap)
- Die stitch
  - 1um transition zone
  - Some die not symmetric
- Maintains 100% scribe space

OR



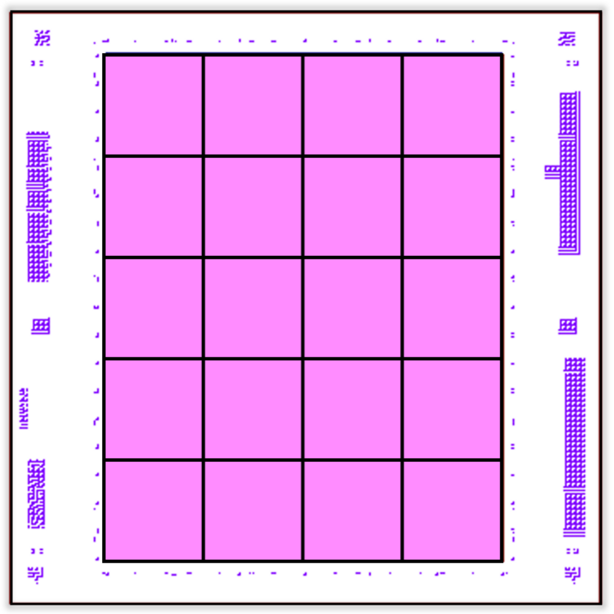
- ~10% throughput loss (more shots)
- Scribe stitch
  - 1μm transition zone
  - Layout flexibility
- X-platform field matching
- Reduces scribe space by >50%

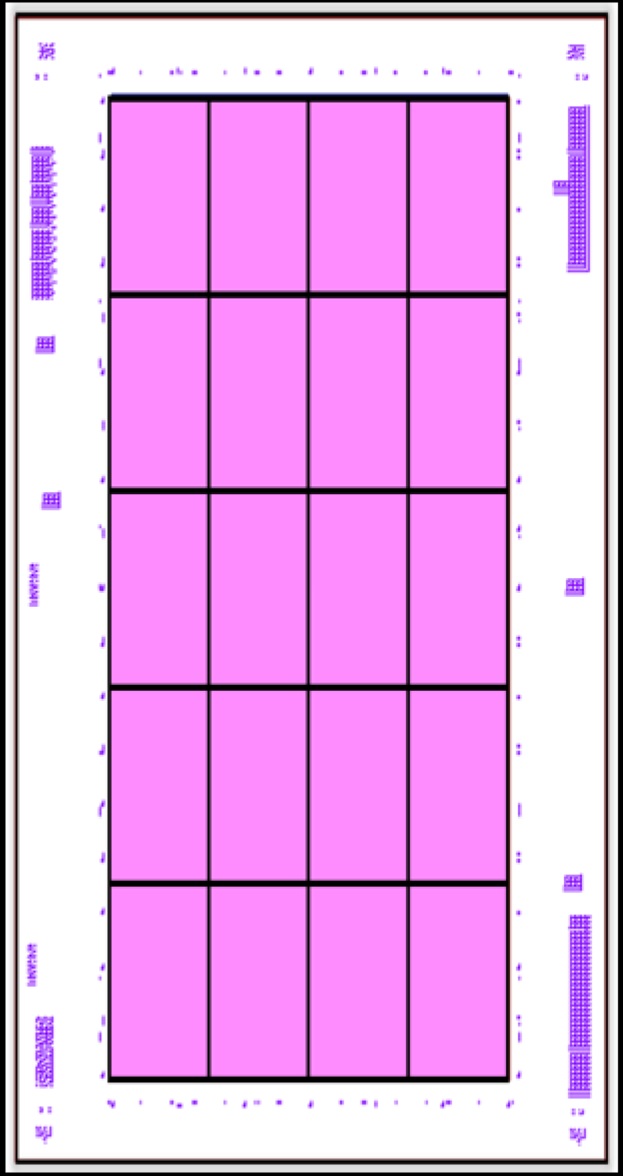
Large Format High-NA EUV Masks

Even after considering Half-Field disadvantages:

- High-NA EUV full-field large format masks' **cost will make them impractical for DRAM applications**
- Expect a few DRAM layers requiring High-NA EUV
- Maskshop tools and mask ecosystem need to be duplicated for large format blanks

Standard Field Mask
6 x 6 inches





Large Format Mask

Thank you!

Acknowledgements
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