5th Annual eBeam Initiative Luncheon
SPIE – February 26, 2013

Aki Fujimura
CEO – D2S, Inc.
Managing Company Sponsor – eBeam Initiative
The eBeam Initiative:

- Is an educational platform for eBeam technology and its impact on all lithography approaches
- Open to any company in the semiconductor design chain with an interest in eBeam technologies
Two Industry Veterans Join as eBeam Initiative Advisors

Hugh Durdan Xilinx

John Chen NVIDIA
New: The Fine Line Video Journal
Use your new earphones!

Winter 2013 Edition

**Shot Talk:**
D₂S

**From the White Board:**
Ryan Pearman

**Tech Talk:**
Samsung & D₂S

**Perspectives:**
Hugh Durdan, Xilinx

\[ eMEEF = N \frac{\Delta CD_{wafer}}{\Delta eBeamDose} \]
Design for eBeam (DFeB) Roadmap

Roadmap Themes
- Mask write times
- Total cycle times
- Mask accuracy
- Wafer quality
- Design for eBeam Methodology

2010
- Complex masks
- Overlapping shots – circles, VSB
- Model-based mask data prep (MB-MDP)

2011
- Thermal analysis of overlapping shots
- Dose control for accuracy
- Double simulation for more accurate analysis of wafer quality

2012
- Mask CD Uniformity improvements
- Accurate measure of mask goodness
- Full chip MB-MDP

2013
- Design for eBeam (DFeB) mask methodology
- Incorporating eBeam Initiative technology roadmap
Wafer Process Enhanced by eBeam

- More Complex Shapes on mask enhance Wafer Process Latitude

- Complex Masks, Manhattanized or ideal curvilinear, had two problems:
  - Poor mask CDU leading to unreliable results on wafer
  - Mask write time

- Samsung and GLOBALFOUNDRIES studies show MB-MDP solves this problem

Source: Samsung and D2S at BACUS 2012
Multibeam Technology Progress

eMET POC exposure with 256k-APS    ILT device test pattern

ILT device test pattern
Design: DNP

<table>
<thead>
<tr>
<th>Scanning Stripe exposure</th>
<th>20nm beam size</th>
<th>5nm pixel size</th>
<th>with PEC</th>
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exposure of DNP design

exposure 2-times smaller

Source: IMS Nanofabrication at BACUS 2012
Our Next Speakers

- **Chip Design Perspective**
  - Hugh Durdan, Xilinx

- **DSA Technology Challenges**
  - Dr. Tatsuhiko Higashiki, Toshiba

- **Q&A**
Lithography Challenges in Advanced Nodes – A Design Perspective

Hugh Durdan
Vice President, Portfolio & Solutions Marketing
The ‘Chameleon’ Chip
Field Programmable Gate Array (FPGA)
**FPGA Characteristics**

- **Large devices**
  - Often > 400mm²
  - Up to 7 billion transistors

- **Regular structures**
  - Ideal for driving process maturation

- **Historically benefitted from Moore’s Law**
  - Insatiable demand for more capabilities & capacity
  - Until 20nM, process scaling has offered higher performance, lower power, and lower cost at each successive node
So What’s Changed?

- More complex transistor structure = more masks
- Double patterning required for finer features in 20nM = more masks
- Net result is 30% increase in masking layers
- Directly translates into increased mask and wafer costs
And Even Worse…

- Mask write time increases exponentially
  - Reduced throughput
  - Higher cost per mask

- More restrictive design rules
  - Larger die

- Reduced CD uniformity
  - More design margin
  - Lower yields
What Happens at 16/14nM?

➤ The Good
  – Higher performance or lower power
    • But not both…

➤ The Bad
  – Interconnect pitch same as 20nM
    • So no die shrink…

➤ The Ugly
  – Even more restrictive design rules
    • Die size could grow!
  – More mask layers
    • Fin-FET structure & double patterning
  – Lower yields
10nM & Beyond: Quadruple Patterning

- "Double Double"
- Extends life of existing infrastructure
  - 193nM light sources & immersion lithography
- Only a stop-gap for 10nM
- Alignment becomes a significant issue
- Even more restrictive design rules
- More masks = increased mask and wafer costs
Other Possibilities Xilinx is Watching

- EUV
- EBDW
- Hybrid Approach
- Directed Self-Assembly
Perspectives

➢ Lithography challenges are a significant threat to maintaining Moore’s Law

➢ Cost per transistor is going up for the first time in the history of the semiconductor industry

➢ No good solution on the horizon
  – Quadruple patterning only good in the short-term
  – EUV immature, expensive, and late
  – Direct-write too slow today for volume production

➢ eBeam will be part of the solution
  – Better accuracy in mask making to reduce CD variation
  – Hybrid approach
  – Direct write if throughput can be improved
DSA Technology Challenges

Center for Semiconductor Research & Development
Advanced Lithography Process Technology Dept.

Tatsuhiko Higashiki
Lithography Challenges

ArF im
NA > 1~1.35

EUVL
NA = 0.32 → > 0.4x ?

EUVL + SADP
EUVL + DSA
ArF im SADP
ArF im SAQP/SAOP ?

ML2
NIL
NIL + DSA
ML2 + DSA

hp56nm
hp43nm
hp32nm
hp2xnm
hp1xnm
hp0xnm

Performance & Economics

SADP: self-aligned double patterning
SAQP: self-aligned quadruple patterning
SAOP: self-aligned octuplet patterning
**DSAL** *(Directed Self Assembly Lithography)*

Lithography of using self-organization phenomenon of polymer

**BCP: block co-polymer**

- **Under layer with guide pattern**
- **Hydrophobic Acrylic styrene**
- **Hydrophilic**
- **Coating**
- **Heating and phase separation**
- BCP aligns with guide pattern
Grapho-Epitaxy & Chemo-Epitaxy


Tada, Macromol.41,9267(2008)
**DSA L for Contact Hole Pattern**

**Process Flow of DSA Lithography**

1. **BCP Coat**
   - Guide

2. **Annealing**
   - Hydrophilic
   - Hydrophobic

3. **Development**

- **BC**
- **P**

- 100 nm images of DSA and BCP.
Example of DPD Simulation

DSA Simulation Model

- Molecular Dynamics
- Coarse Grained Model by DPD (Dissipative Particle Dynamics)

Available Free Software Tools are:
LAMMPS/GROMAX/OCTA-COGNAC,

\[ m_i \frac{d^2 r_i}{dt^2} = F_i = \sum_{j \neq i} \left( F_{ij}^S + F_{ij}^C + F_{ij}^D + F_{ij}^R \right) \]

F_{ij}^C, F_{ij}^R depend only on \( r_{ij} \) (distance between particle i and j)

Top-down
PS-b-PMMA
Top
Sidewall
Bottom
X-section

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Leading Innovation
### DSA Simulation Model

**Model**
- **Self Consistent mean Field**
  - Based on statistical field theory
- **Dissipative Particle Dynamics**
  - Based on Newton's motion equation

**Challenge**
- **Modeling of thermal fluctuations**
- **Difficult to fit to a measured data**

**Prediction Accuracy**
- Shroedinger's Equation etc
- Rigorous Model
- Impractical model

**Speed**
- (5nm)
- TAT (? years/10μm²)
- TAT (5h/10μm²)
- TAT (1m/10μm²)

**Target**
- (<0.25nm)

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**Needs drastic improvement !!**
Conclusion: Challenges for DSAL

• High performance DSA material
  – Resolution, LWR/LER, Etching
• Long term stability
  – Robust material and tool for environmental control such as surface energy stability, temperature, humidity, pressure and PH, etc.
  – Defectivity, CD and overlay accuracy
• Metrology & Inspection
  – Metrology for 3D profile
  – Inspection technology for 1xnmhp and beyond needs to overcome t-put vs accuracy/sensitivity trade-off.
• Development of molecular dynamics based DSA simulator
  – More accurate simulation model
    • BCP and related molecular design
    • Microphase separation (2D/3D)
    • DSA and guide patterning (litho/wet/dry)
  – TAT vs accuracy trade-off
• DSA OPC/DFM technology
  – Design rule verification
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Thank you for attending!

Q & A