Design For E-Beam Using Talus on a 65nm Test Chip

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D₂S, Inc. and the eBeam Initiative

- Founded March, 2007
- Headquartered in San Jose, CA
- Dev. office in Shin-Yokohama, Japan
- Round A in 2007, led by Benchmark
- Completed Round B in March, 2009

- 10/08 : D₂S-Fujitsu/e-Shuttle collaboration
- 01/09 : D₂S-Vistec/ST/CEA/Leti collaboration
- 02/09 : eBeam Initiative launched with 20 companies including D₂S and Fastrack (www.ebeam.org)
Fastrack

• Fastrack Design is a *Premier Design Services* company.

• We strive to provide industry leading design solutions by staying in the bleeding edge technologies
  – First tapeout in 2002
  – Implementation flow exclusively based on Magma tool suite

• Our goal is to offer the best return on our customers’ investments by providing unparalleled ASIC design services
DFEB enables Maskless All-Layer SoC Prototypes

Design Data

DFEB library and Stencil Mask

E-beam Direct Write

Mask (Reticle)

Stepper

Wafers

OPC

Mask Manufacturing Test & Repair
CP shoots complex features in one shot

Electron Gun

1\textsuperscript{st} Aperture

2\textsuperscript{nd} Aperture

Demagnification

Variable Shape Beam (VSB)

Character Projection (CP)

(4 shots)

(1 shot)

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DFEB Decreases Required Shot Count

- Makes EbDW practical for low volume prototypes
DFEB Designs Can Also Be Made with Mask

DFEB Library

D2S DFEB Methodology

Stencil

E-Beam Processing

Mask Data Prep.

Mask Mfg. Test & Repair

Mask

Photo Processing

RTL

Synthesis, Place & Route

Verification

GDSII

E-Beam direct write path

Conventional photo mask path

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65-nm Test Chip

- Target for 65-nm low-power, 7-metal layers process
- Approximately 3+ Million gates
- Chip size is 4.2 X 8.4 mm²
- Voltages are 1.2V for core, and 3.3V for IO
- Clock frequencies are 166Mhz and 162Mhz
- Designed using DFEB library as much as possible
- Shot count reduction of 10X
Test Chip DFEB flow overview

D2S DFEB 65-nm Library

RTL.v

Synthesis

DFEB.gv

RTL D2S DFEB Shot Count Estimator

Post-Synthesis D2S DFEB Shot Count Estimator

D2S DFEB Methodology

DFEB Lib. Prep.

fix time

Floorplanning

fix cell

fix clock

fix wire

fix drc

TC.gv

TC.dspf

TC.gds

LEC

STA

DRC/LVS

Post-Layout D2S DFEB Shot Count Estimator

Talus

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DFEB Methodology Considerations for Talus

• Implement using DFEB cells to maximize for shot count reduction
  – 158 DFEB overlay cells are built from existing standard cells library
    > Strongly prefers north/flip-south orientations
  – DFEB cells Include memory cells for maximizing memory macros shot count reduction
    > Memory macros strongly prefers north/south orientations

• Force “hide” the conventional standard cells initially, but re-introduce anytime in the flow to fix area, performance and power
  – DFEB and conventional standard cells orientations can be relaxed also

• Optimizing for shot count reduction with DFEB cannot compromise the quality of results
Talus with DFEB was very easy

• Default Talus flow scripts efficiently handled DFEB methodology

• No custom modifications were required, except for floorplanning and power planning
  – It is the same with any SoC design
Floorplan: Test Chip

Fixed footprint of 4.2 X 8.4 mm²

Use non-buffer blockage to:
1) Relieve congestions
2) Tighten utilization
   a) Reduced cell area
   b) Shorten wire lengths
   c) Easier timing closure
Power Planning: Meshes and Chip View

Power/Ground mesh are spaced between 400-500 tracks

Mesh view

Power/Ground rings are wider
Metal widths are integer multiple of 1um

Full chip power plan
## Timing Validation

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>Input Timing</th>
<th>Test Chip Achieved</th>
<th>% diff</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Specification</td>
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<td></td>
</tr>
<tr>
<td></td>
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</tr>
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- In a single pass, Talus correlates very well with Third Party sign-off tools
Power and IR Drop Met Requirements

Total power: 422.8mW
Leakage: 27.1mW
Internal: 132.6mW
Swcap: 263.1mW

Data activity factor = 0.2
Clock activity factor = 0.5

Max. IR drop: ~29.4mV
VDD: 15.2mV
VSS: 14.2mV
@(2043.6um, 3367.88um)
DFEB Shot Count Estimation

- Shot count is added as an optimization criteria to area, performance, power, and yield
- D²S DFEB methodology optimize shot count through
  - co-design of the cells and the stencil mask characters
  - synthesis, place and route flow
- D²S DFEB Shot count estimation is available in every stage of the design
  - Similar to timing analysis, there is successive refinement of the estimate
- Cost of manufacturing with EbDW is directly related to shot count, even more than area
DFEB Test Chip Shot Count Estimation Report

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- Shot count estimation at Post-synthesis stage provide more conservative reduction ratio
- Shot count estimation at Post-Layout stage provide more refined estimate
- Estimation is based on metal 1, contact, poly and diffusion
Talus Met Our Expectation

- No customization scripts required
- Met our area, performance, and power goal
- Single pass timing correlated well with third party tools
- Reduced turnaround time compared with Blast Fusion
Conclusions

• DFEB with Talus is very easy
• Met our 10X shot count reduction goal
  – Without compromising area, performance and power
• Silicon validation is expected later in 2009
• DFEB enables maskless all layer SoC prototype
Q&A