Introducing
The eBeam Initiative

20 Charter Members & Advisors Across the Ecosystem

Jan Willis
eBeam Initiative Facilitator
Why Industry Collaboration?

- Removes barriers to adoption of design for e-beam (DFEB)
- Increases investment in multiple supply chains
- Inspires leadership

More designs, Faster Time to Market
## eBeam Initiative Roadmap

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<th>Initiative Launch</th>
<th>Design Proven</th>
<th>DFEB Certification</th>
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<td>• &gt;10 members, advisors&lt;br&gt;• Website and papers</td>
<td>• 65-nm test chip&lt;br&gt;• Methodology guide&lt;br&gt;• 45-nm test chip</td>
<td>• Design certification training</td>
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### Timeline

<table>
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<tr>
<th>Year</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2011</th>
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<td><strong>Semi-annual member meetings with advisors</strong></td>
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### Manufacturability Proven

- 65-, 45-nm and 32-nm proof points
- On-going effort for each node

### Multiple Chip Suppliers

- Design kit availability
- Equipment readiness
Today’s Agenda

Industry Need for DFEB

Aki Fujimura, CEO - D2S, Inc.
Managing Sponsor – eBeam Initiative

Fujitsu Viewpoint

Shinichi Machida, President and CEO - Fujitsu Microelectronics America
Steering Group – eBeam Initiative

eSilicon Viewpoint

Jack Harding, Chairman and CEO - eSilicon Corporation
Design Team Advisor – eBeam Initiative

Summary and Q&A
Industry Need for DFEB

Aki Fujimura
CEO - D2S, Inc.
Managing Sponsor - eBeam Initiative
Mask Cost is Top Concern

Source: Global Semiconductor Association (GSA) member survey, December 2007
Enabling the Long Tail of SoCs

The long tail

Source: Chris Anderson’s “The long tail: Why the future of business is selling less of more”
The Tail is Getting Shorter

We can enable the tail with DFEB

Revenue per Design

Cost of Manufacturing Chips per Design

Big opportunity

# of Designs

Non-addressable market

32-nm with mask
40-nm with mask
65-nm with mask

Maskless SoC

Big opportunity
The Derivatives Opportunity

10x reduction in mask cost increases derivatives by 10x

Ratio of Revised to New Designs

Reticle ASP

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Fast EbDW using CP
Available today and uniquely effective at and below 65-nm

ELECTRON GUN

1\textsuperscript{ST} - APERTURE

2\textsuperscript{ND} - APERTURE

DEMAGNIFICATION

(A) VSB: Variable Shaped Beam

(B) CP: Character or Cell Projection

Drawing Courtesy Hitachi High-Technologies
EbDW Underutilized
Even with CP due to throughput

Comparison Source: D2S Computer simulation of e-beam write time on a particular test case (speed up is dependent on aperture size and utilization %)
DFEB Breakthrough
Makes CP EbDW practical for low volume

Comparison Source: D2S Computer simulation of e-beam write time on a particular test case (speed up is dependent on aperture size and utilization %)
Collaboration Already Underway

- Fujitsu, e-Shuttle and D2S to Prove DFEB Design and Manufacturing
- 65-nm low-power test chip
- Announced October 2008

Pictured are (left to right) **Dr. Haruo Tsuchikawa**, President of e-Shuttle, **Hiroyuki Asahida**, Director of Marketing at Fujitsu Microelectronics, and **Aki Fujimura**, Chairman and CEO of D2S.
Today’s Proof Point at SPIE

• CEA/Leti, Advantest, and D2S joint paper at 2:20 p.m., Session 5: EBDW

• Manufacturing proof of accurate CP projection for 32-nm contacts
Summary of Today’s News

• 20 charter members launch the eBeam Initiative
• Initiative roadmap established
• Execution already underway
• Design test chip in 2009
• Today’s SPIE paper proves manufacturability at 32-nm
• With DFEB, direct write has arrived