

# ILT and Curvilinear Mask Designs for Advanced Memory Nodes

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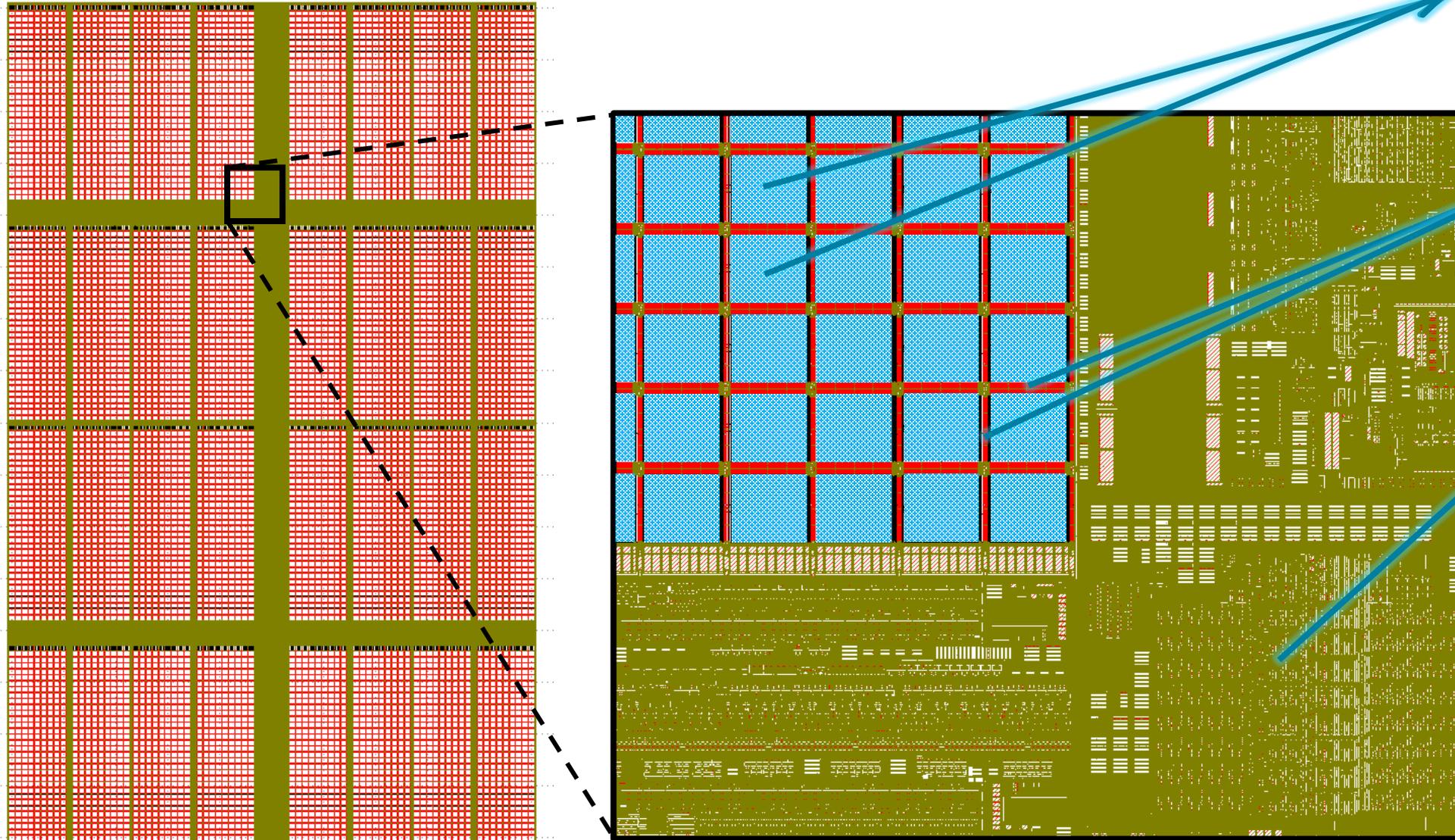
# Outline

## ILT and Curvilinear Masks use cases in Advanced Memory Nodes

- ILT use cases in memory designs
- Hot-Spot ILT correction and retargeting
- Why curvilinear masks, why now?
- DRAM Array Core ILT use case
- DRAM Contact layer full-chip curvilinear ILT

# Memory Architectures: DRAM Designs

Different use cases of ILT in Memory Designs



Memory Element:  
- Array core

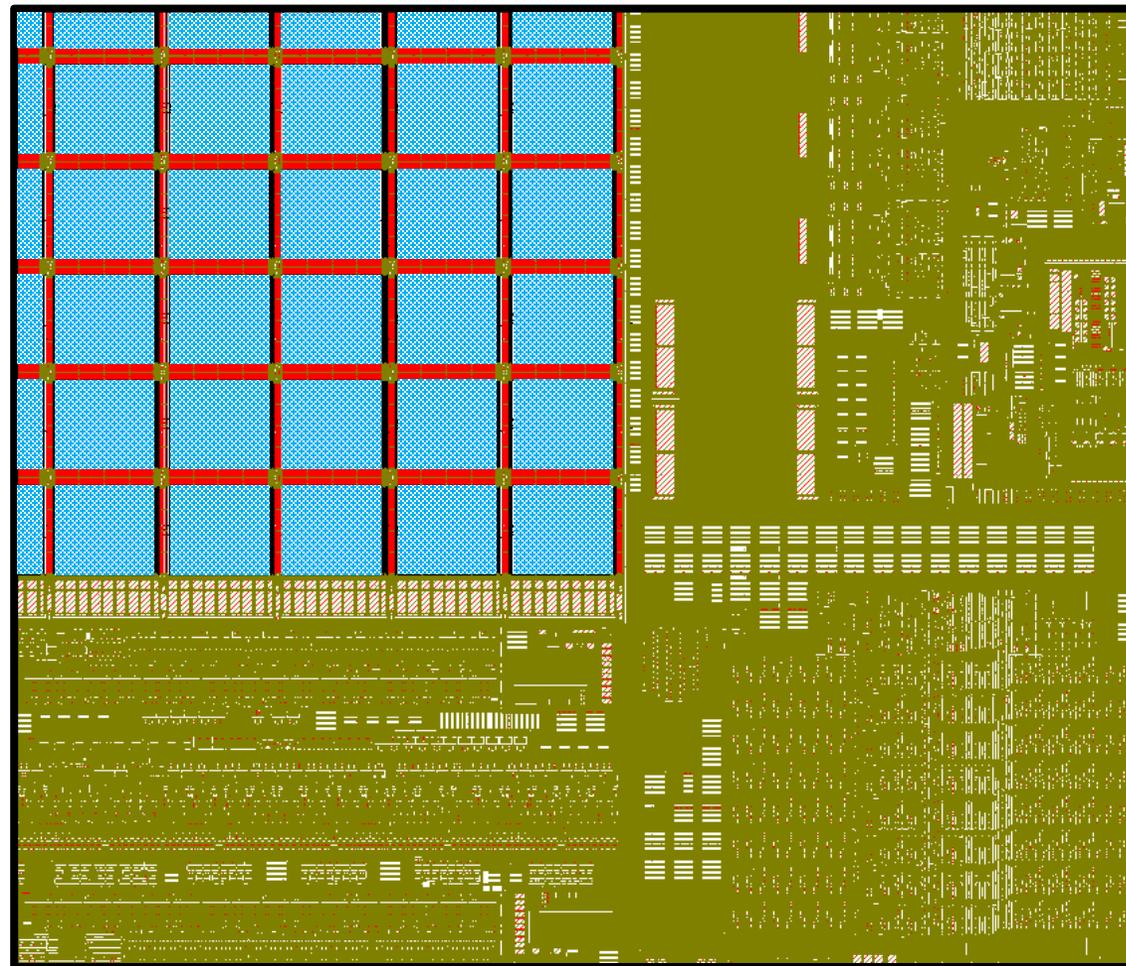
Read / Write:  
- Sense Amp  
- Row Driver

Periphery Circuit:  
- I/O  
- Power  
- Repair

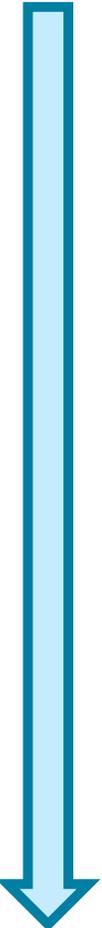
# ILT on Memory Devices

Different ILT use cases in Memory Designs

Increasing ILT  
and Mask  
Complexity

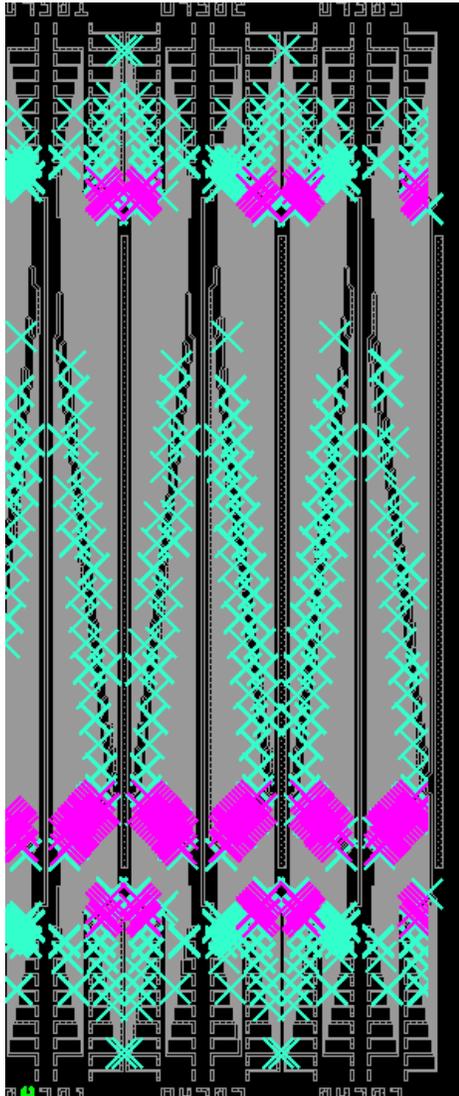


- **Repair Flow**
  - Applied on verification “*hot spot*” areas only
- **Memory Array Core**
  - Highly repetitive, can leverage hierarchy. Center of Core doesn’t change
  - Edge of Array Core changes based on surroundings → Correction needed
- **Array Read / Write**
  - Highly repetitive. Custom design (DTCO)
  - Dense layout, little space for SRAFs
- **Periphery Only**
  - Metal routing layers
  - Interconnect layers
  - Little repetition to leverage, large amount of SRAFs
- **Full-Chip**
  - Includes all of the above



# ILT use cases in NAND Routing Layer: Hot-Spot Repair

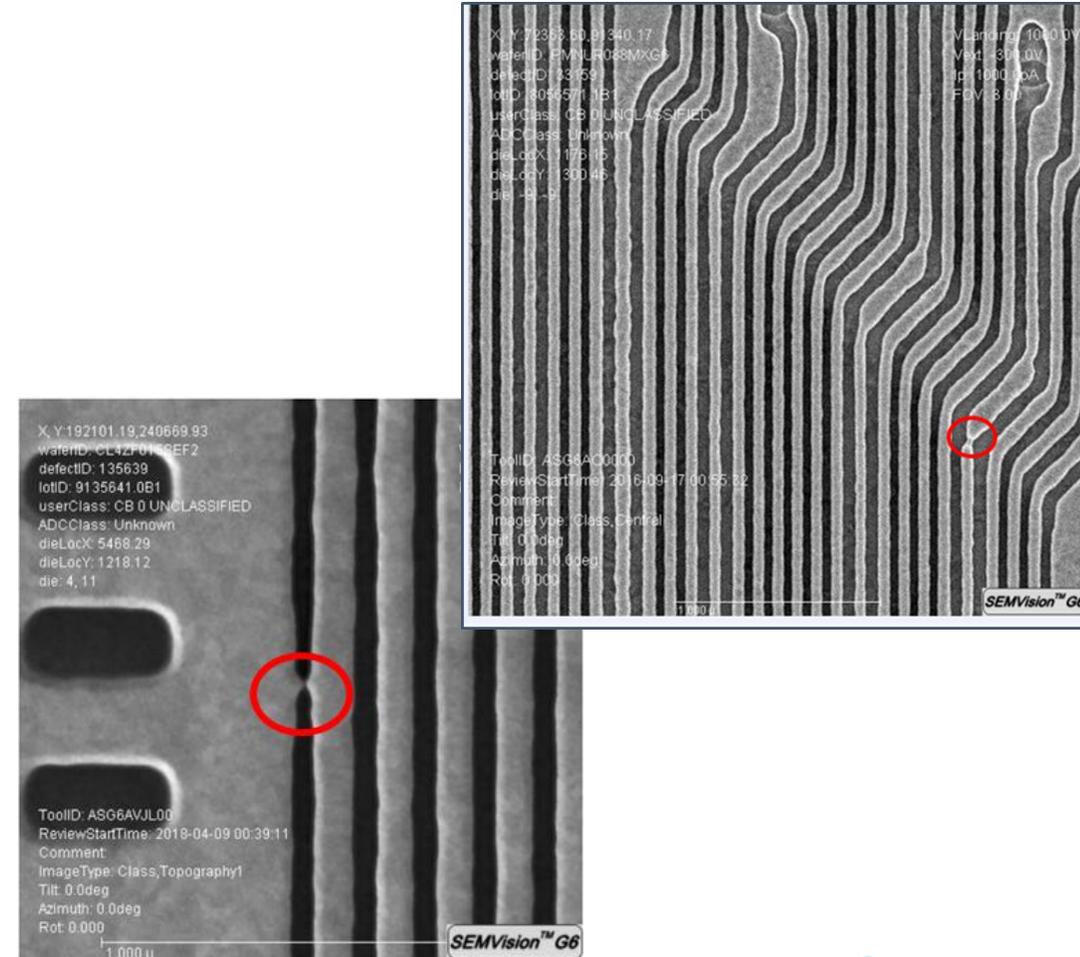
Hybrid ILT and conventional OPC with blending



Aggressive scaling and large topography in 3D NAND architecture, requires addition DoF budget in routing layers

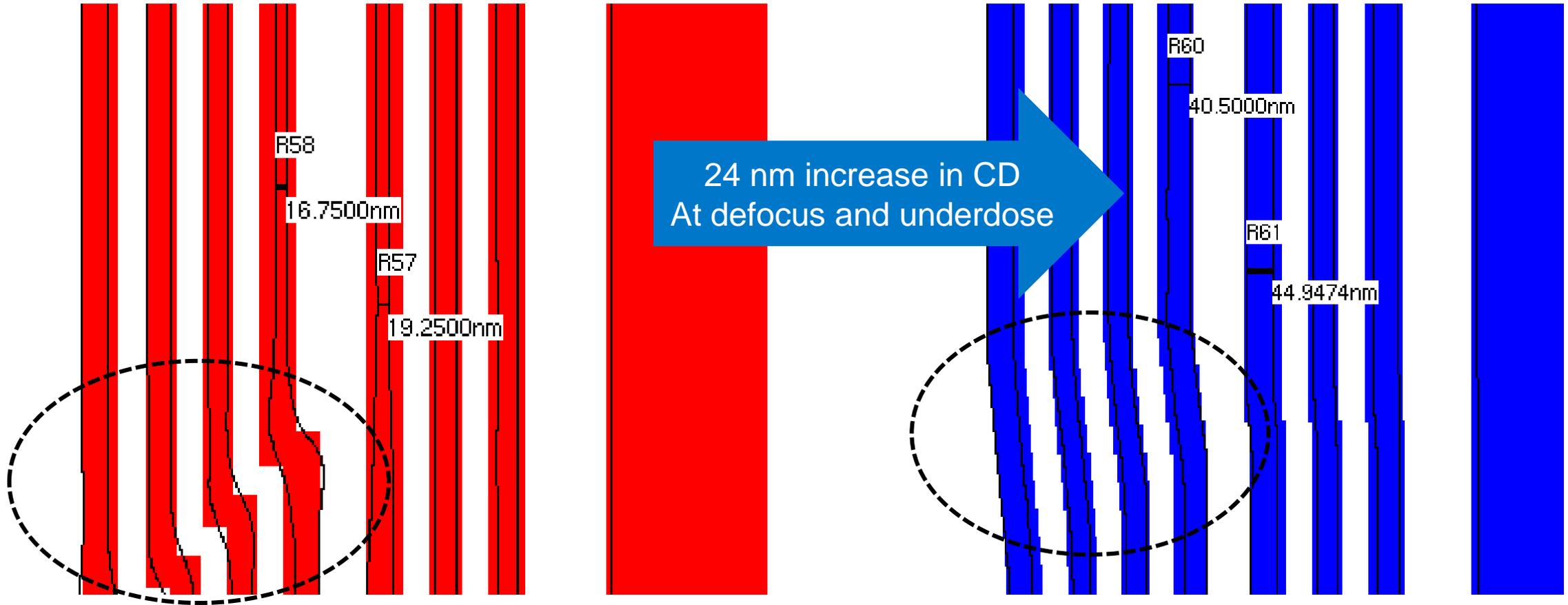
- **Green** "X" are pinching sites
- **Pink** "X" are bridging sites
- All weak spots are located near:
  - transition from vertical to horizontal
  - transition from vertical to 45-degree line
  - edge of dense line regions

Limited PW – First to fail sites



# Jog and Edge Progression ILT Optimization

CD increases by 140% on the weakest location at defocus and underdose condition

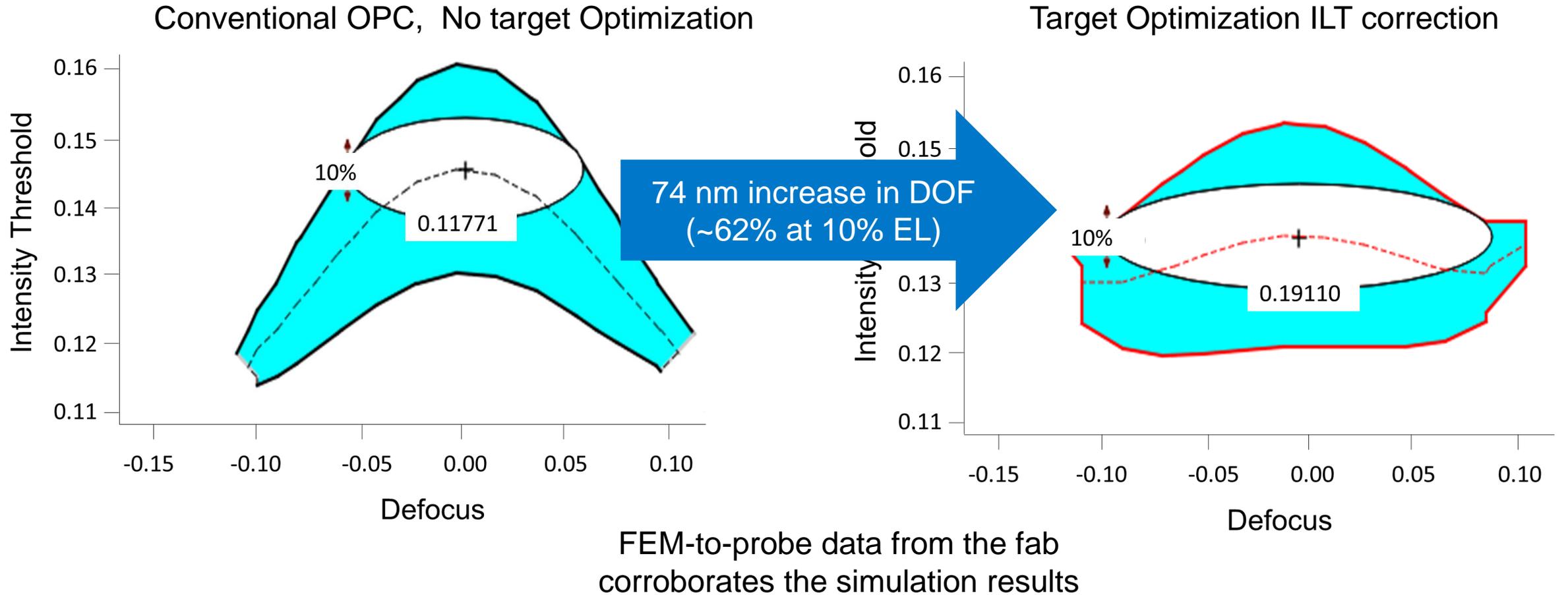


Conventional OPC, No target Optimization

Target Optimization ILT correction  
Straight Jogs converted to *smooth* transitions

# Jog and Edge Progression ILT Optimization

Depth of focus increases by 62% with jog and edge progression optimization



# Why Curvilinear?

## Improved Process Window

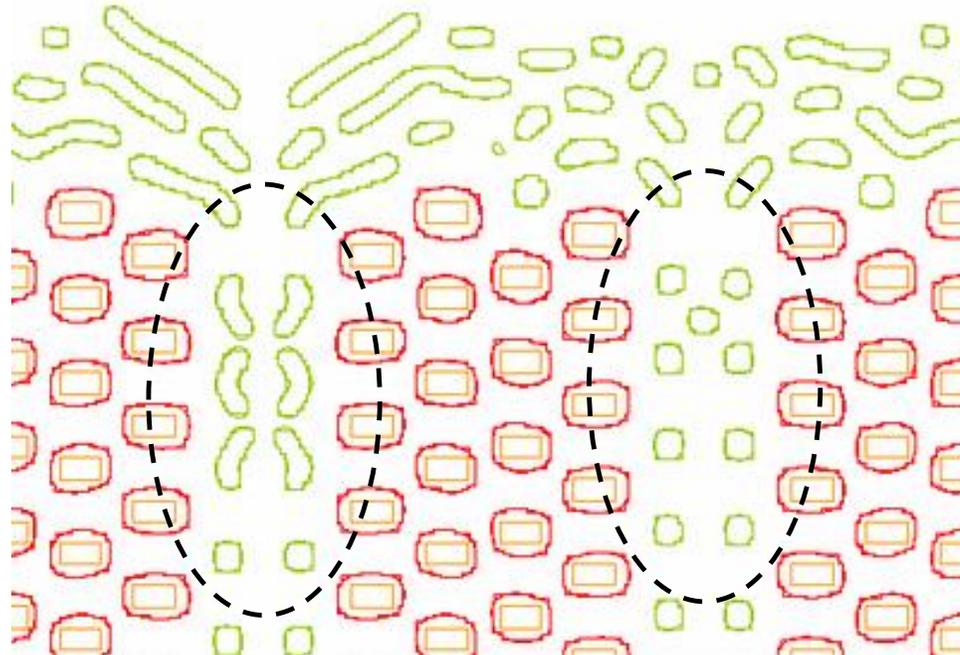
- Optimal AF placement

## Faster ILT

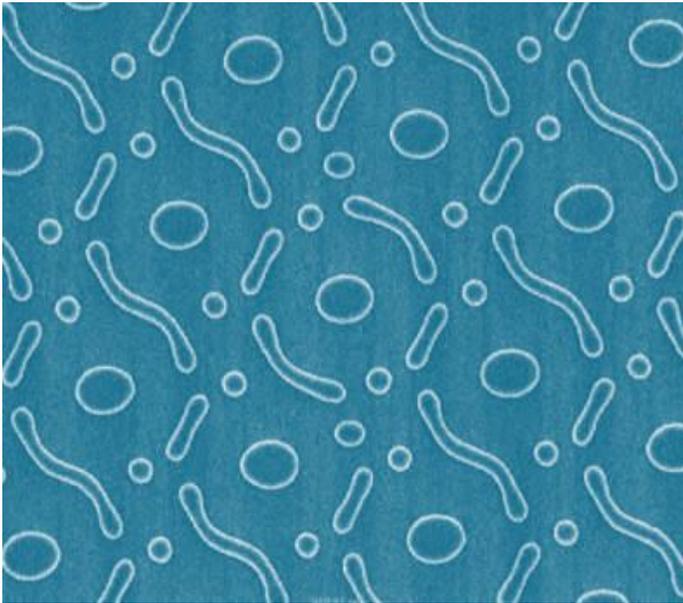
- No Manhattanization step saves time
- Up to 50% time reduction

## Consistency

- Higher degree of consistency by skipping Manhattanization



# Curvilinear Masks



## VSB Single Beam Mask Writers

- Fracture step required to convert curvilinear shapes to polygons (VSB “shots”)
- Long write time and small shots → high variability, contribute to mask and wafer CD uniformity variation

## Multi-beam Mask Writers

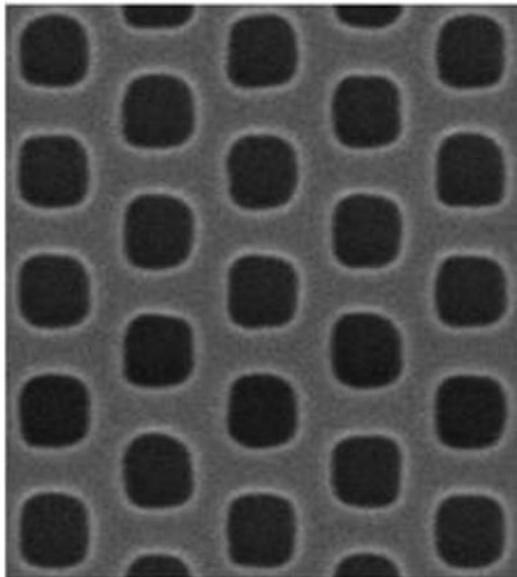
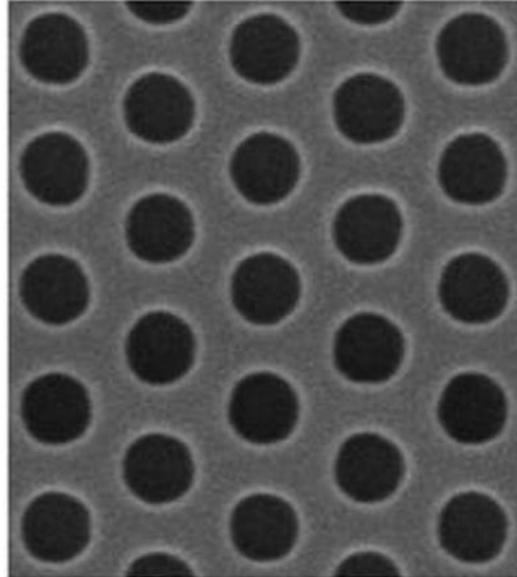
- Constant write time, independent of mask density and complexity
- Not limited by shot size, mask written as “pixels” (grey scale)
- Curvilinear masks show demonstrated higher degree of wafer CDU uniformity

# Curvilinear Masks: DRAM Array Layer

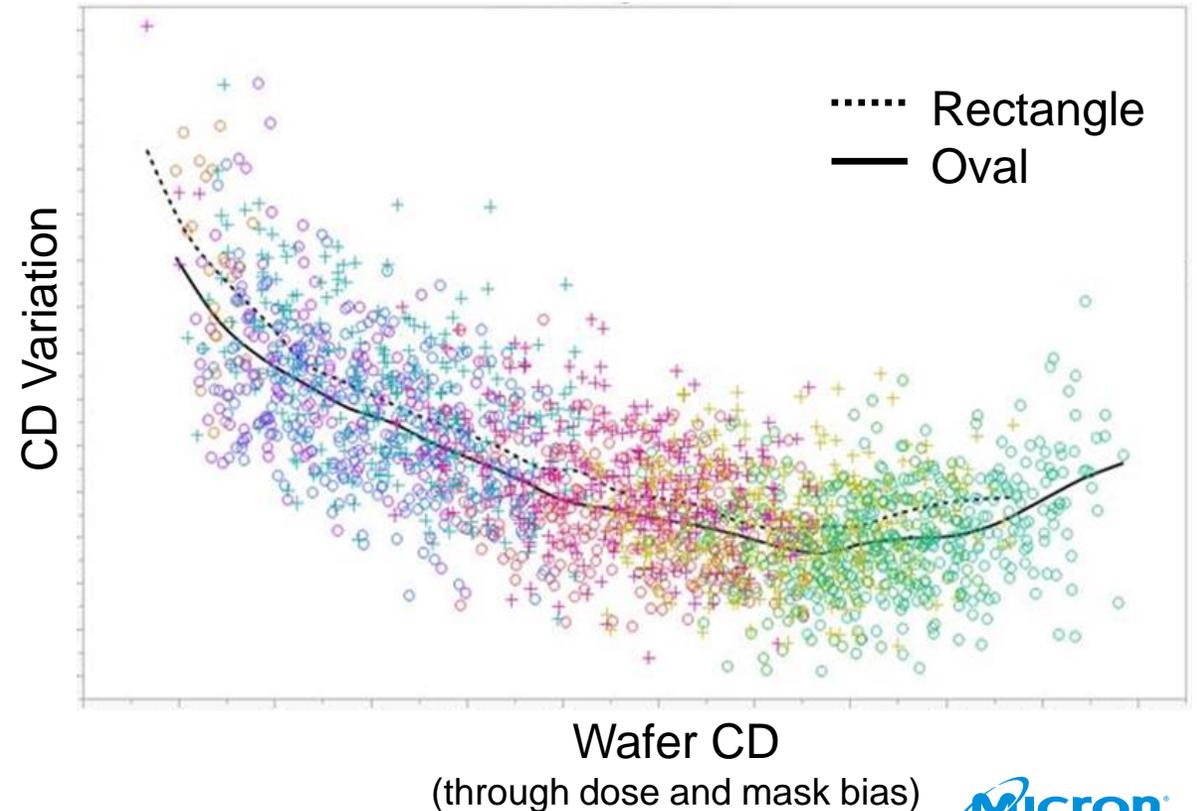
Mask Data



Mask SEM



- Curvilinear DRAM Array shapes produced visually more consistent shapes
- Wafer CD Uniformity shows a ~10% improvement for curvilinear mask



# Curvilinear Masks

## Additional Benefits

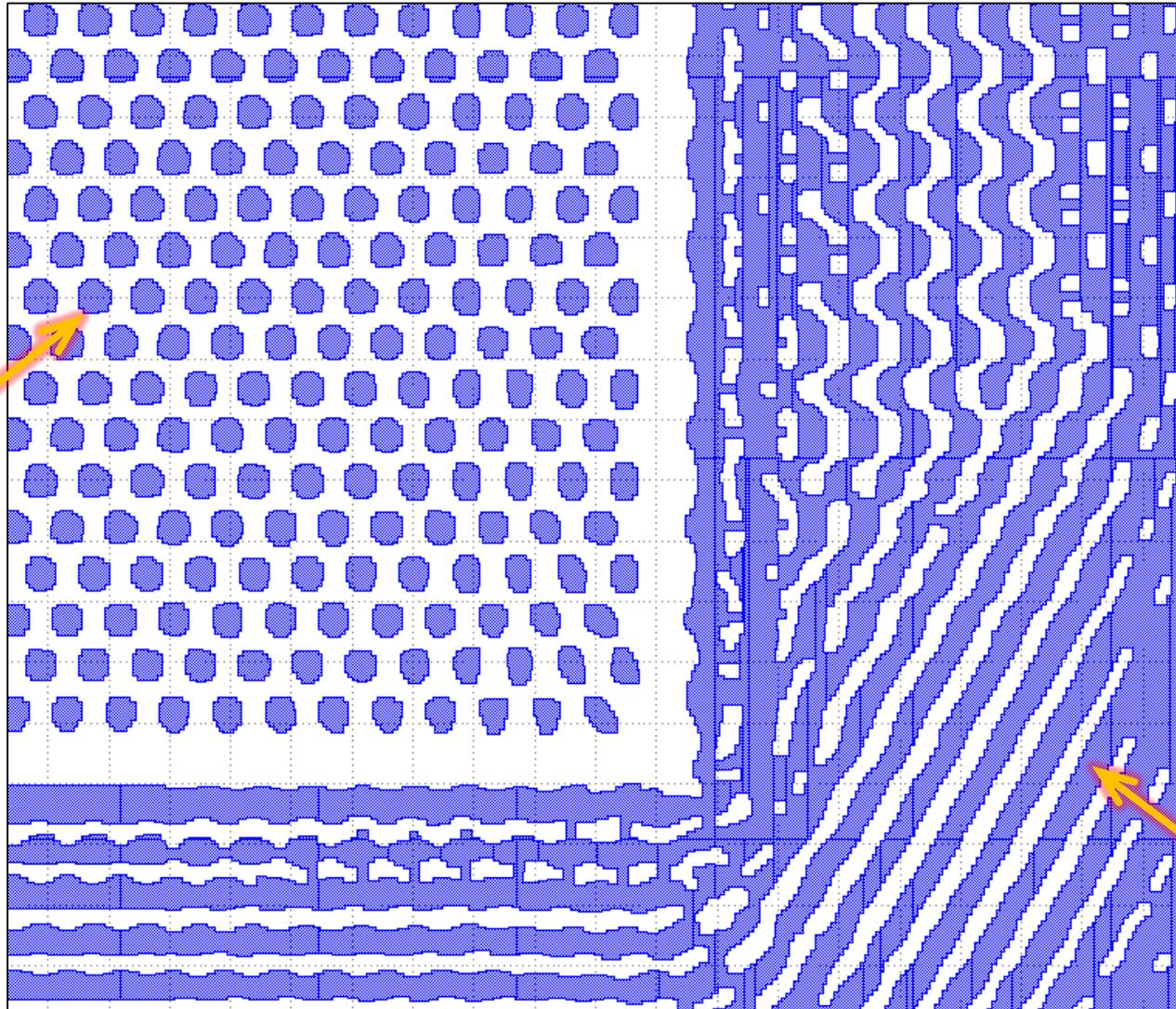
- More accurate OPC models
  - No need to compensate for differences between “intended” shape and mask shape

## Challenges

- EDA infrastructure not fully supporting curvilinear mask files
  - Efficient file format
  - Layout tools support
  - MRC compliance checks with curvilinear operators
- Database to Mask reticle inspection could be challenging

# DRAM Array Core: Curvilinear ILT Correction

Improved NILS, CD Uniformity, and Contact Shape



## Full-Chip ILT

- Application to a common DRAM array contact-like layer
  - CD uniformity and contact shape is critical

## Mask Complexity

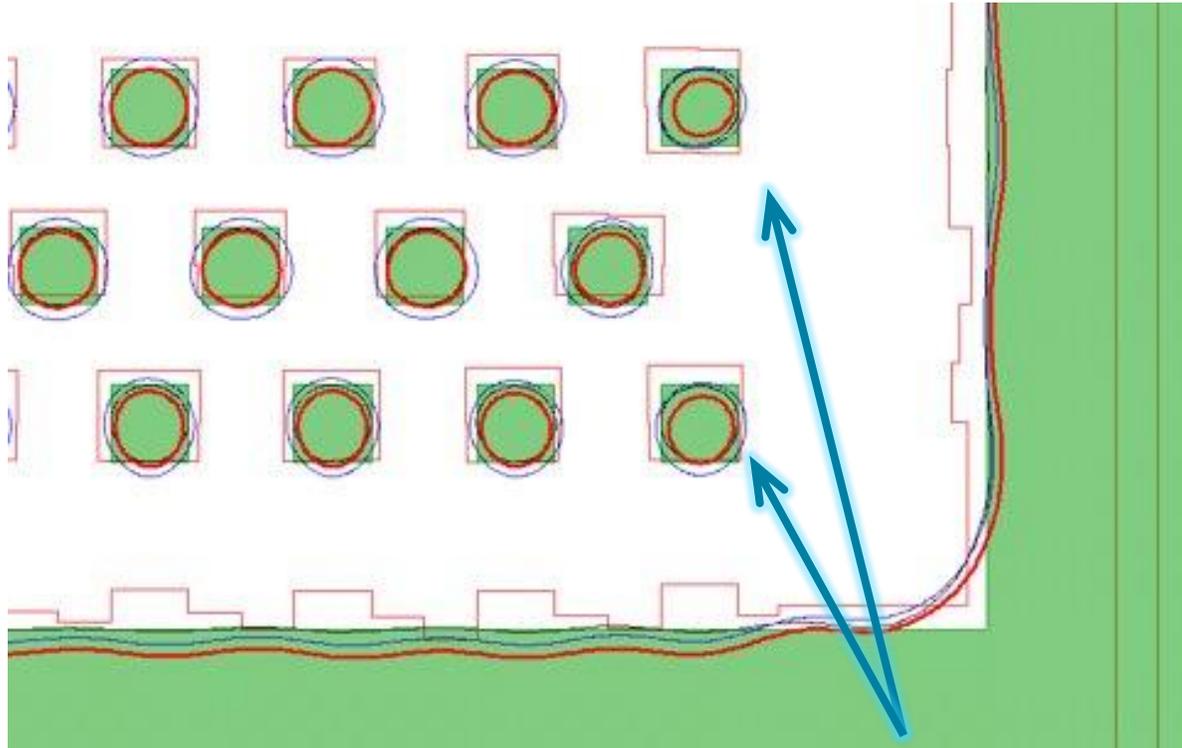
- Both Main features and assist features are curvilinear (small step Manhattanized) ILT

Assist Features (SRAFs)

# DRAM Array Core: Full-Chip ILT

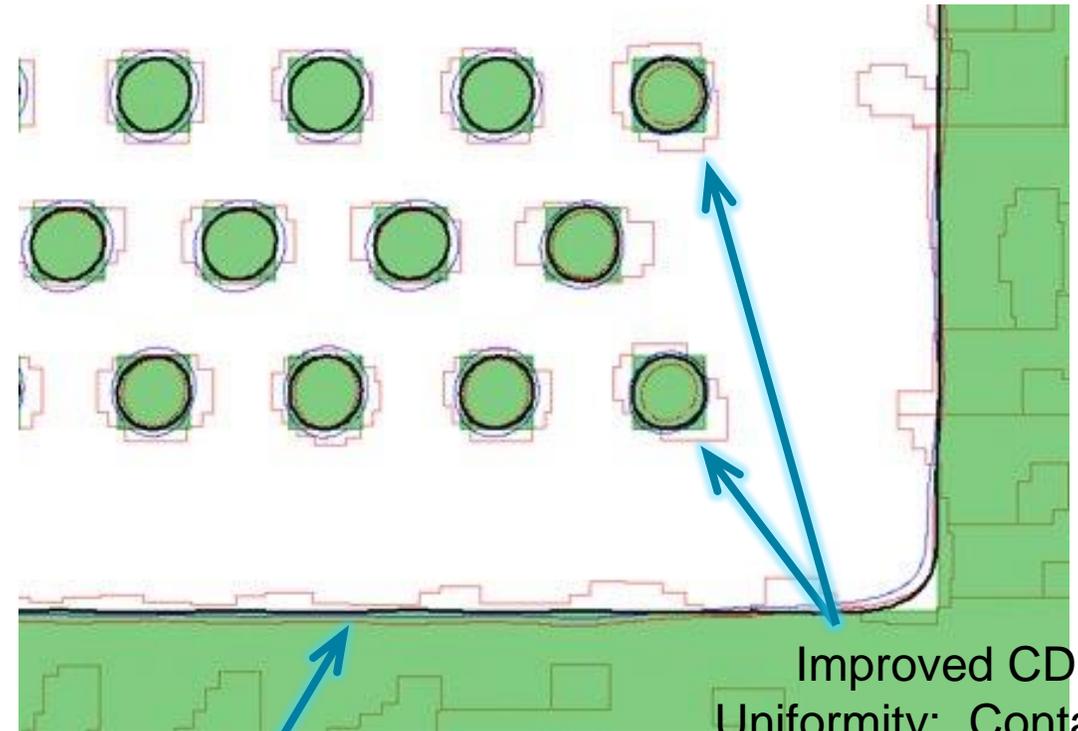
Improved pattern fidelity and NILS across PW conditions

Conventional OPC (hand-based)



Contacts lose their shape at off-nominal conditions

Full-Chip ILT

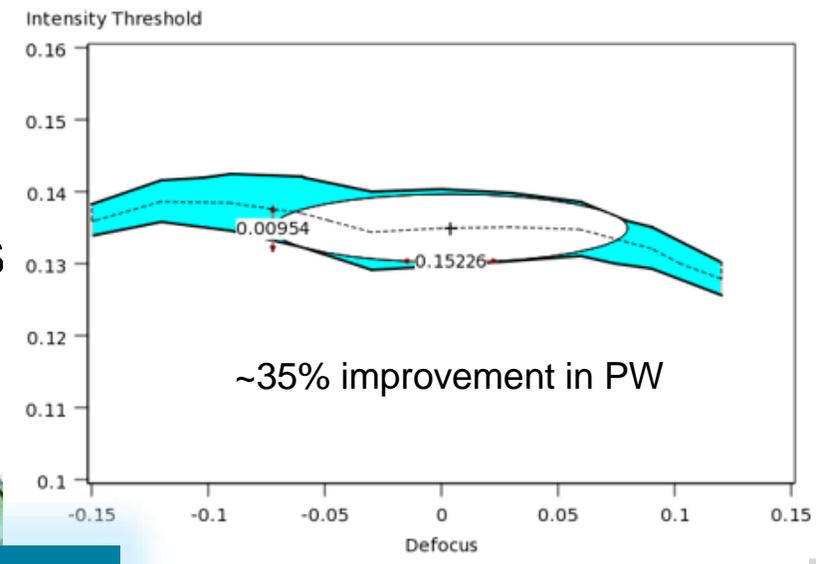
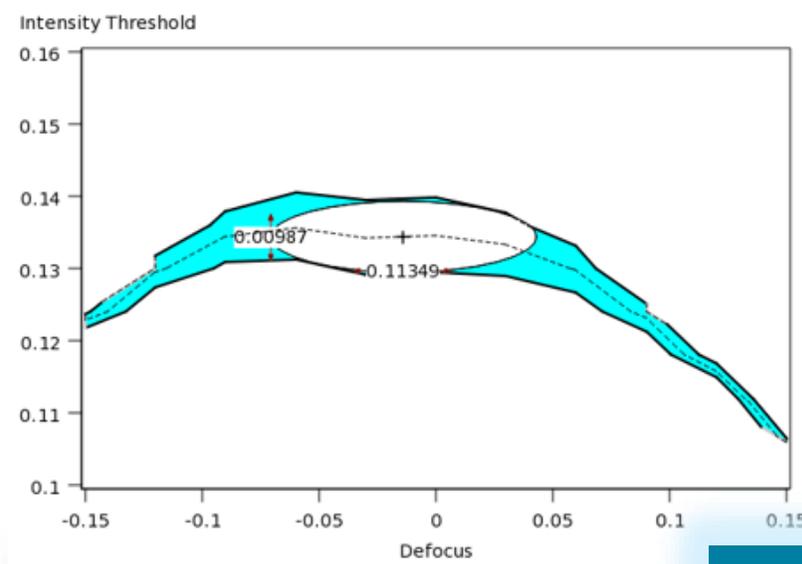


Straighter edge at off-nominal conditions

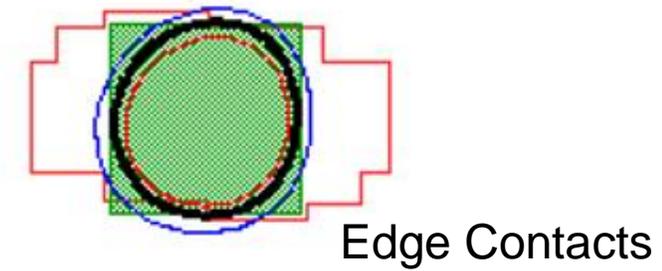
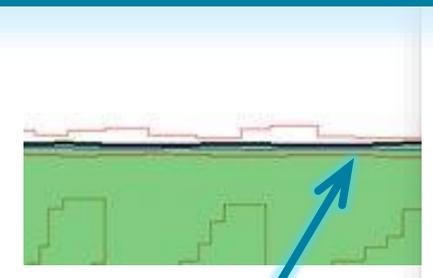
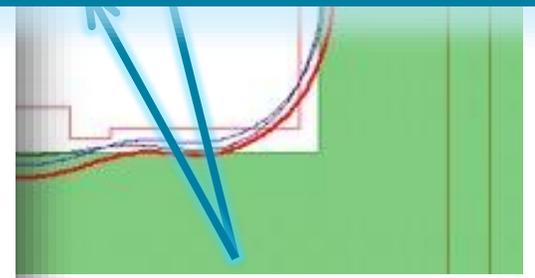
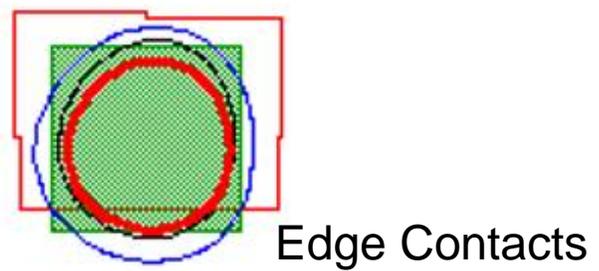
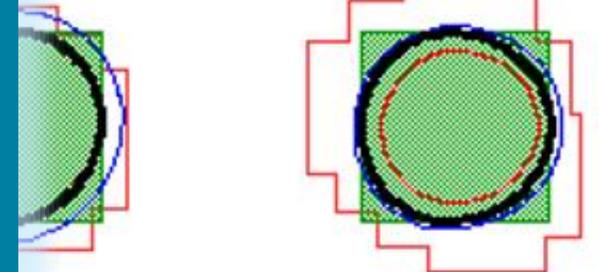
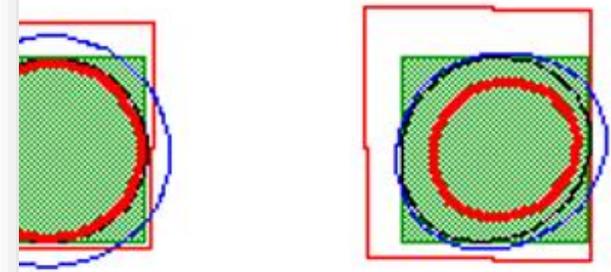
Improved CD Uniformity: Contacts stay round through process window

# e: Full-Chip ILT and NILS across PW conditions

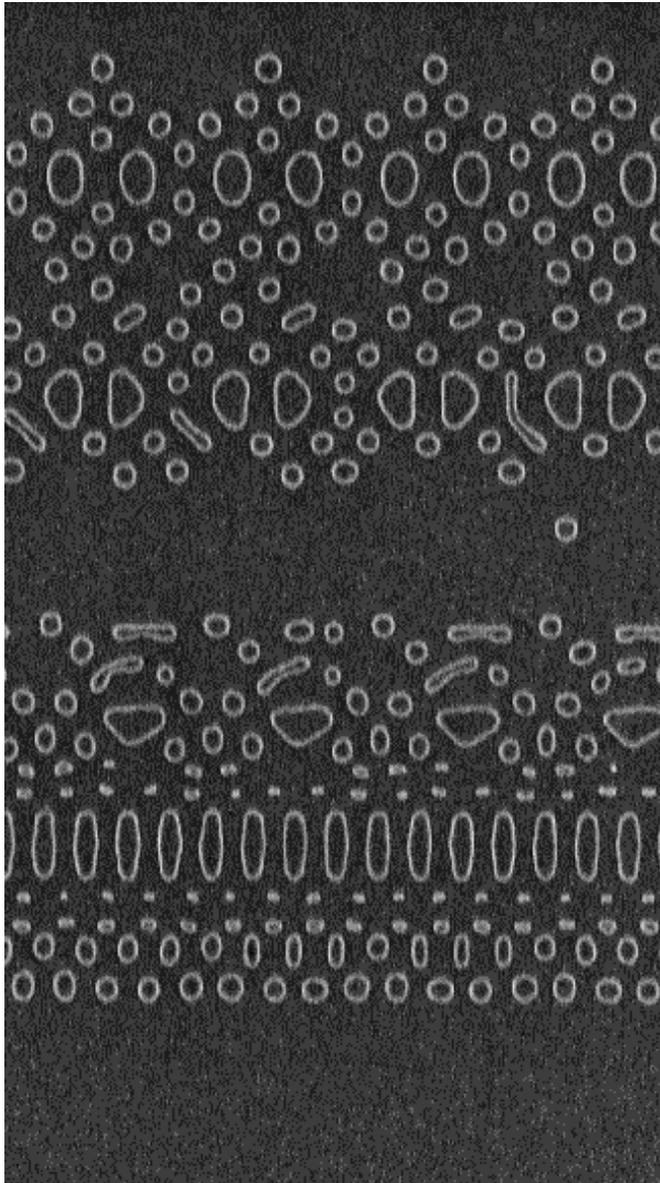
(based)



Co-optimization of AFs and Main Feature are necessary to maximize CD Uniformity and Process Window  
 → ILT

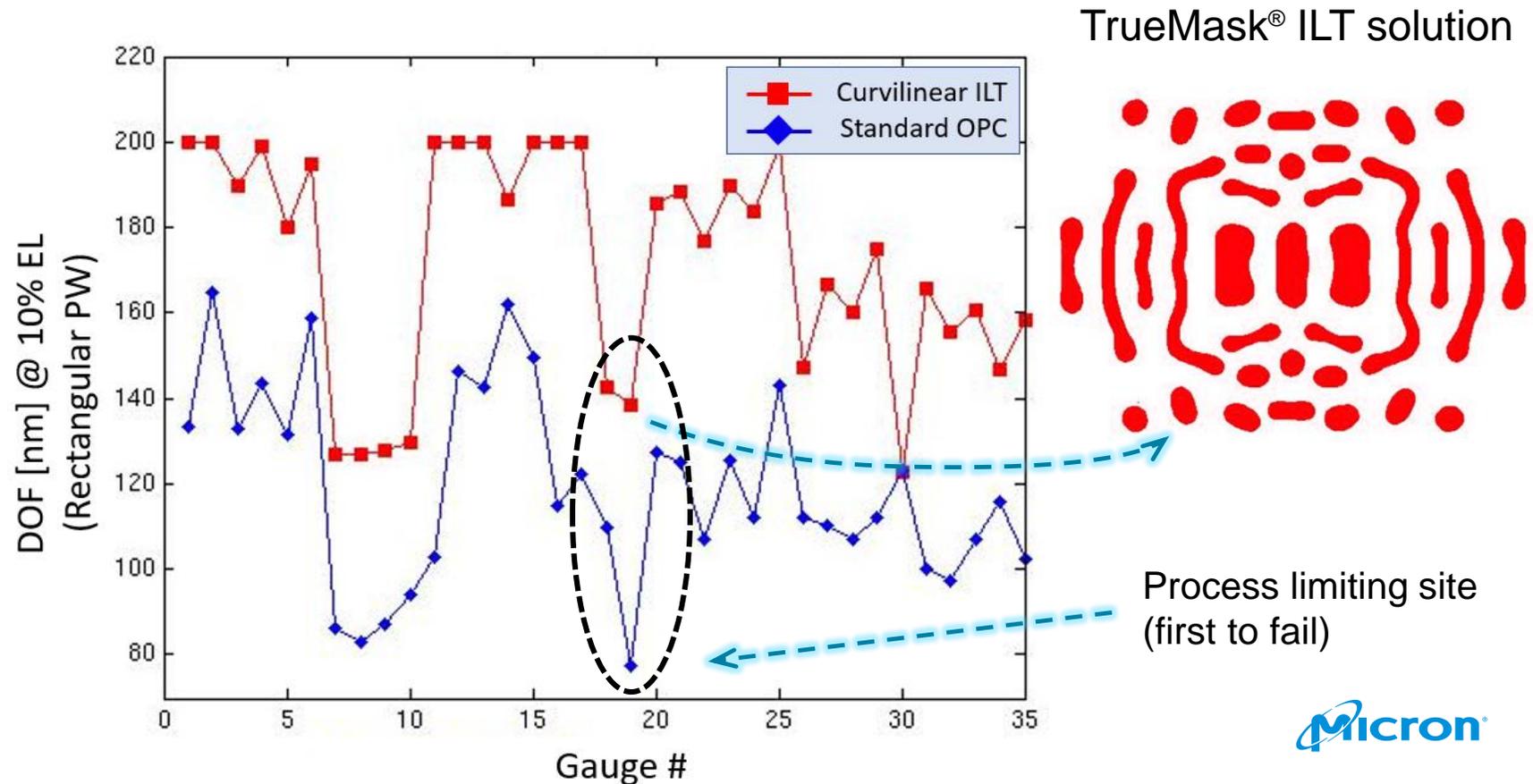


# Full-Chip ILT: DRAM Interconnect Contact Layer



## Curvilinear ILT compared to regular OPC

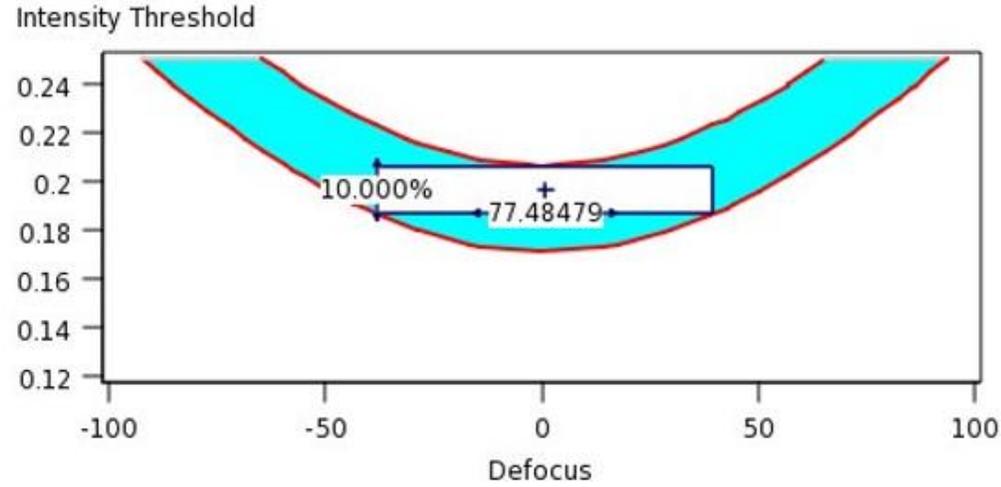
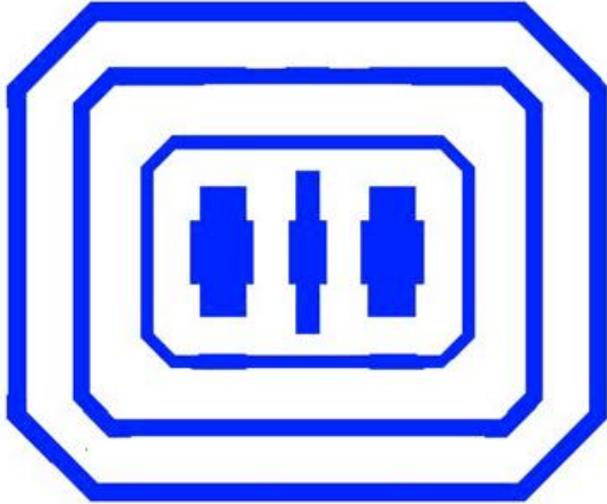
- Process Window limiting sites show significant improvement with curvilinear ILT



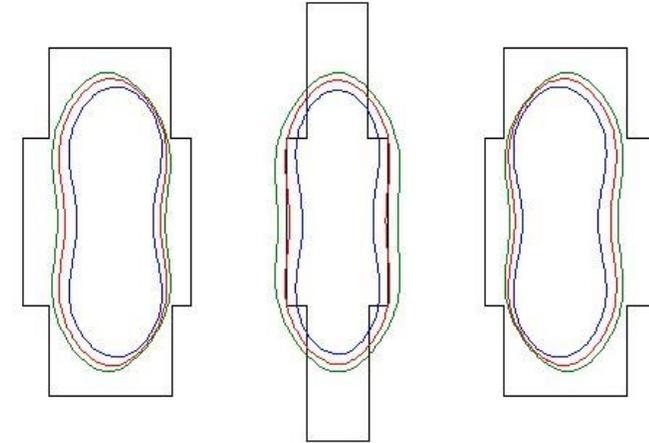
# Process Window Comparison: DRAM Contact

Curvilinear ILT vs. Standard OPC: *First to fail site*

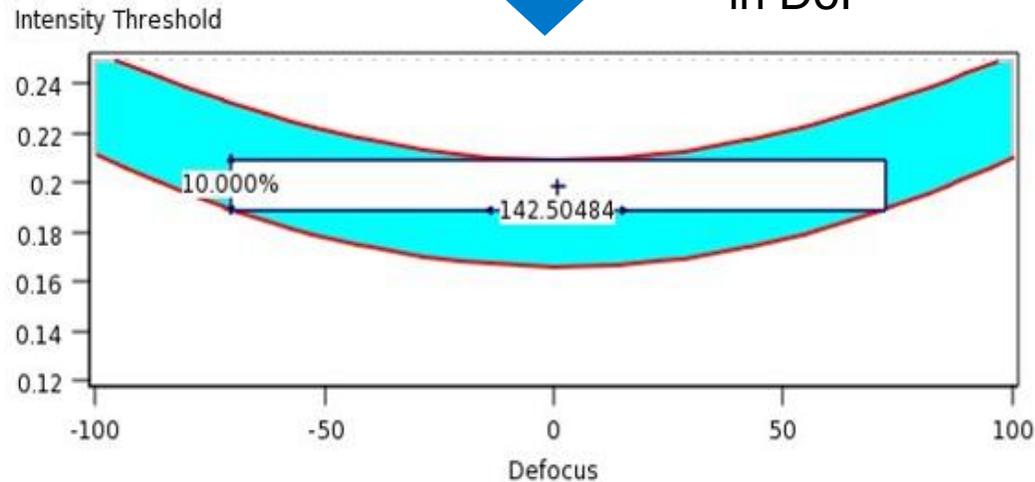
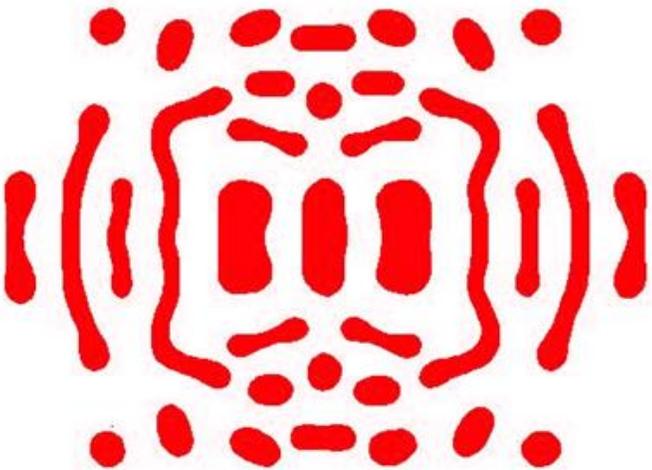
Standard OPC



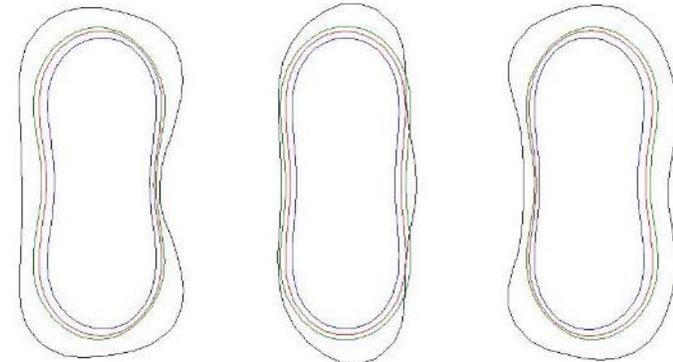
PV Band  
0, 60, 90nm defocus



Curvilinear ILT

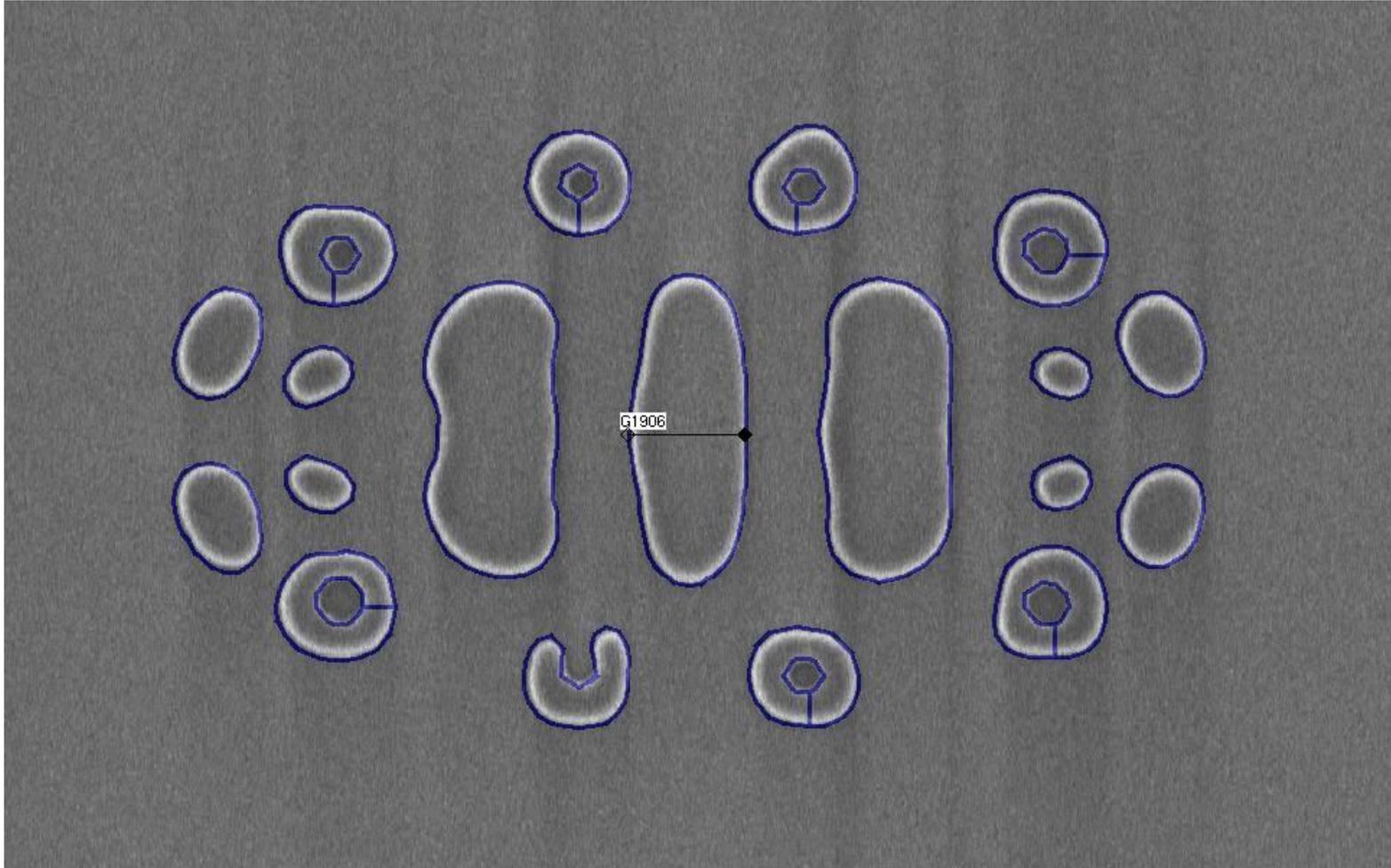


~85% increase  
in DoF



# Curvilinear Mask Pattern Fidelity – MBMW

Overlay of Mask Data and Mask SEM

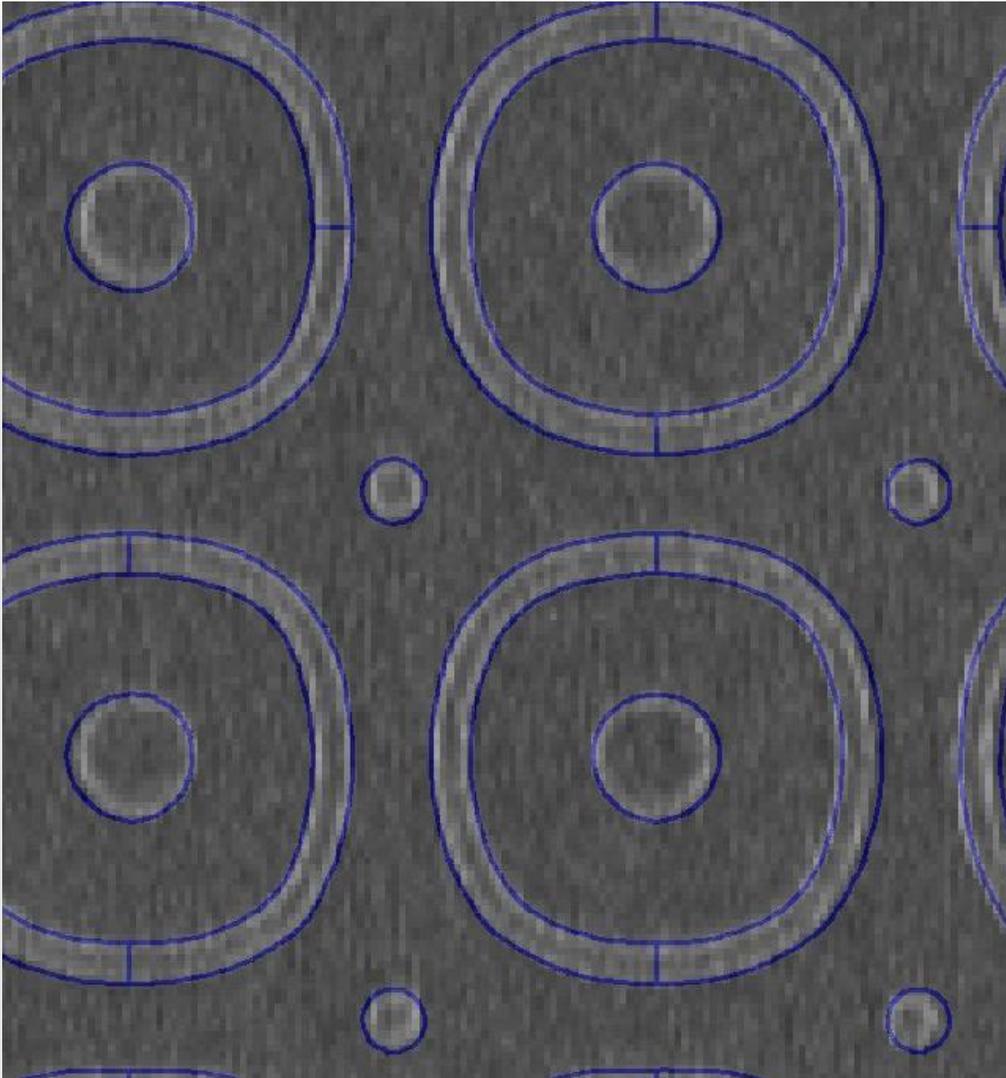


Blue outline = Mask Data

- Pattern fidelity is not a concern, even with aggressive AFs
- In collaboration with NuFlare and D2S: written on MBM-1000

# Curvilinear Mask Pattern Fidelity – MBMW

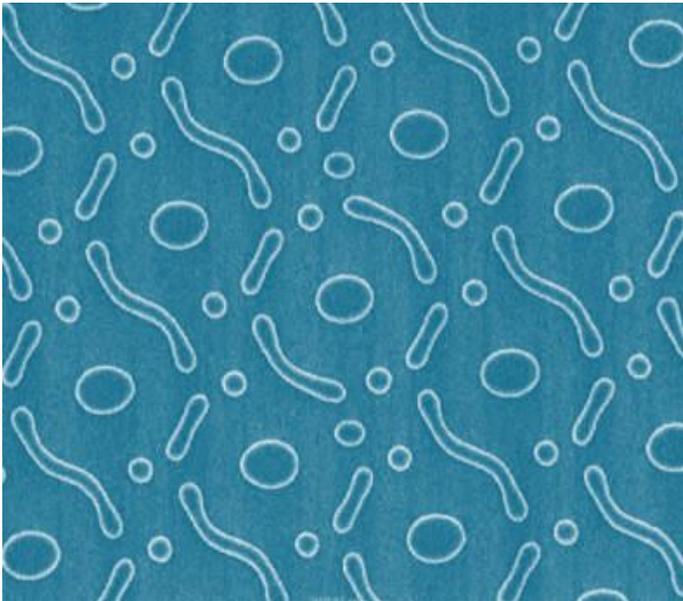
Overlay of Mask Data and Mask SEM



Blue outline = Mask Data

- Pattern fidelity is not a concern, even with aggressive AFs
- In collaboration with NuFlare and D2S: written on MBM-1000

# Conclusions



## Curvilinear ILT

- Offers a means to increase process window on critical layers in memory designs
- Enables the extension of immersion lithography and multi-patterning
- Helps improve wafer CD uniformity

## Curvilinear Masks

- With the introduction of multi-beam mask writers, curvilinear masks are possible today
- Some challenges still exist in handling full-chip curvilinear data

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