



The Resurgence of ILT

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Synopsys, eBeam Initiative Member

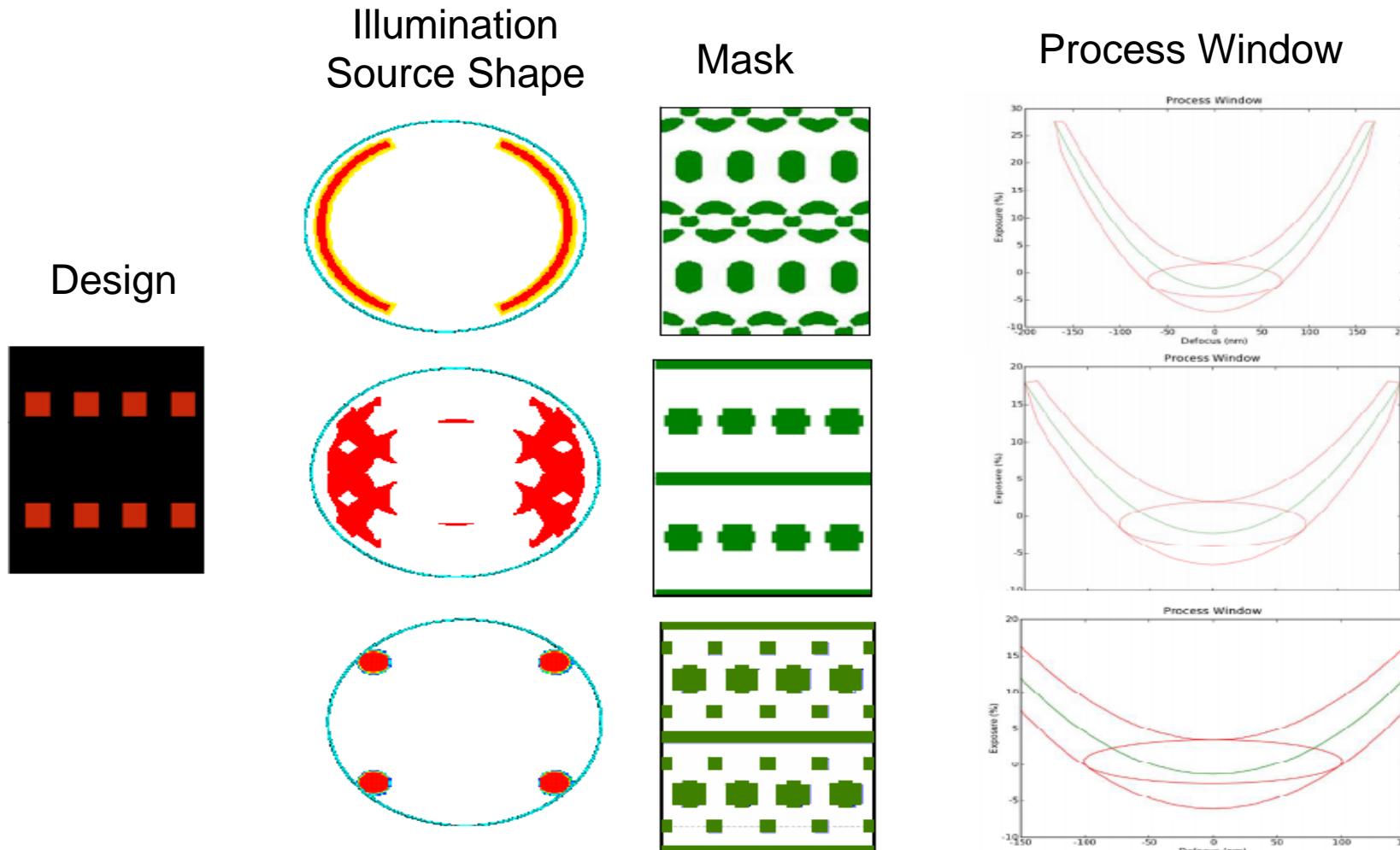


Outline

- ILT Overview
- ILT Use Cases
- ILT Future Extensions

ILT Overview

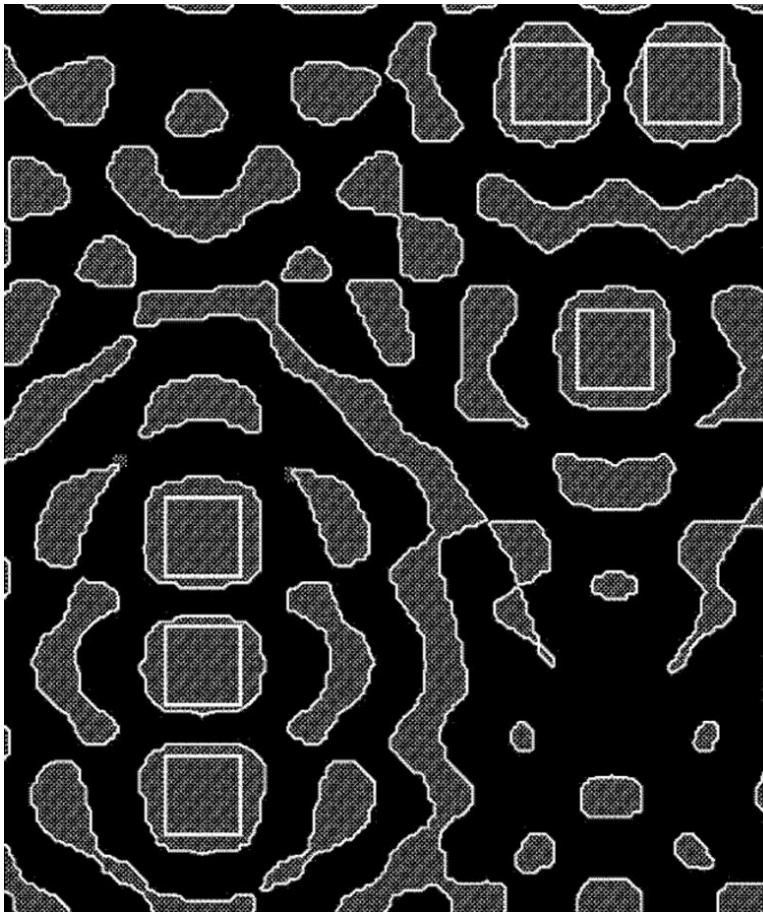
Why do we need ILT? Sensitivity to Illumination Source Shape



Validation of inverse lithography technology (ILT) and its adaptive SRAF at advanced technology nodes - art. no. 69240T
Article (PDF Available) in Proceedings of SPIE - The International Society for Optical Engineering
6924 · March 2008

Why do we need ILT? Sensitivity to Local Design Variation

- Interaction range from design edge to AF is measured in hundreds of nm
- Uniquely capturing this in a simple rule table of AF distances from design edges is difficult/impossible



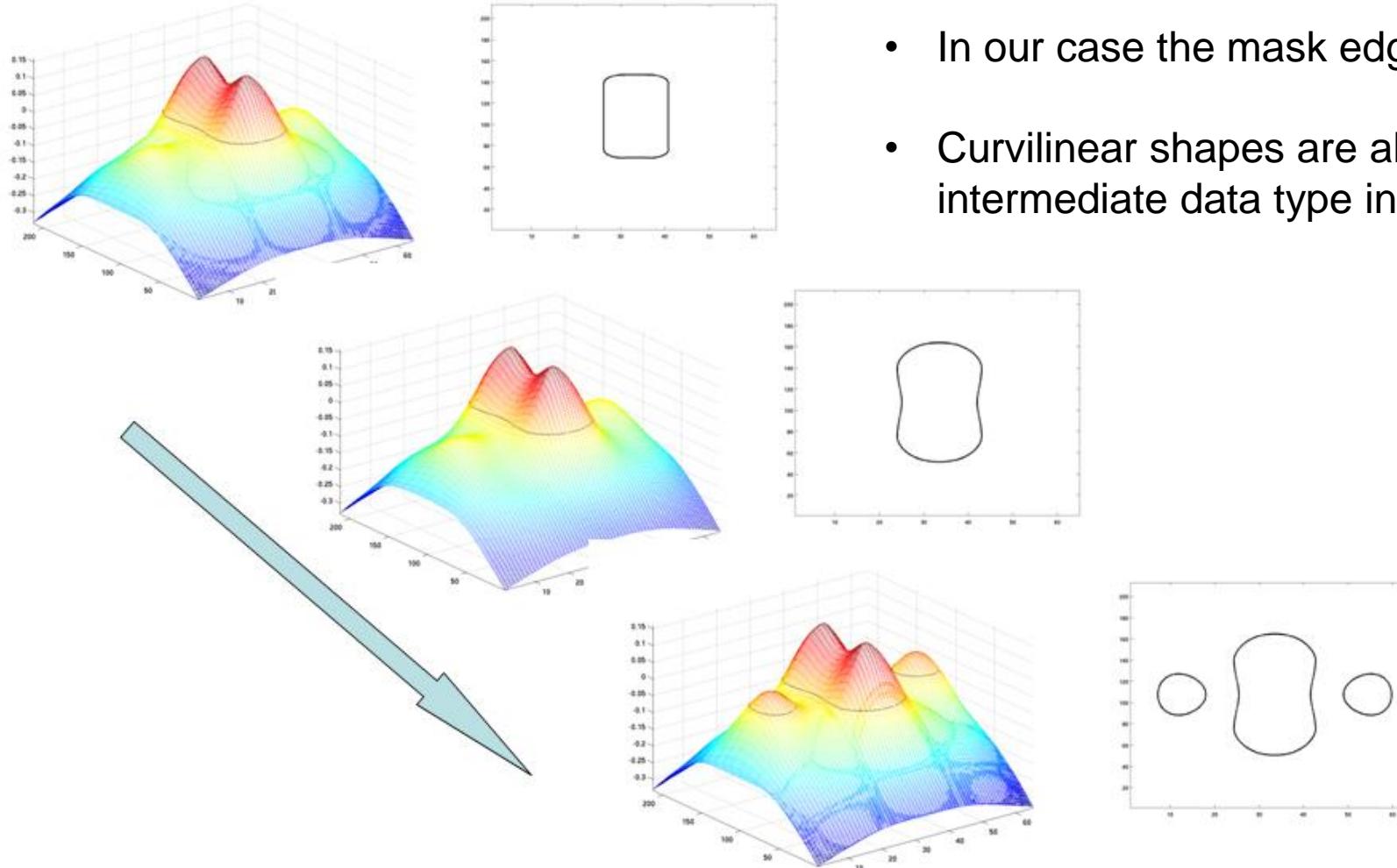
Inverse lithography for 45-nm-node contact holes at 1.35 numerical aperture
[Monica Laurel Kempsell](#) ; [Eric Hendrickx](#) ; [Alexander Trichkov](#) ; [Kyohei Sakaiiri](#) ;
[Kenichi Yasui](#) ; [Susuki Yoshitake](#) ; [Yuri Granik](#) ; [Geert Vandenberghe](#) ; [Bruce W. Smith](#)
[\[+\] Author Affiliations](#)

J. Micro/Nanolith. MEMS MOEMS. 8(4), 043001 (November 18, 2009).
doi:10.1117/1.3263702

- Also, sensitivity to other complicated short range effects:
 - CPL
 - EUV complications, e.g. mask 3d, anamorphic, etc.

ILT Levelset Optimization

Optimization Driven Mask Creation

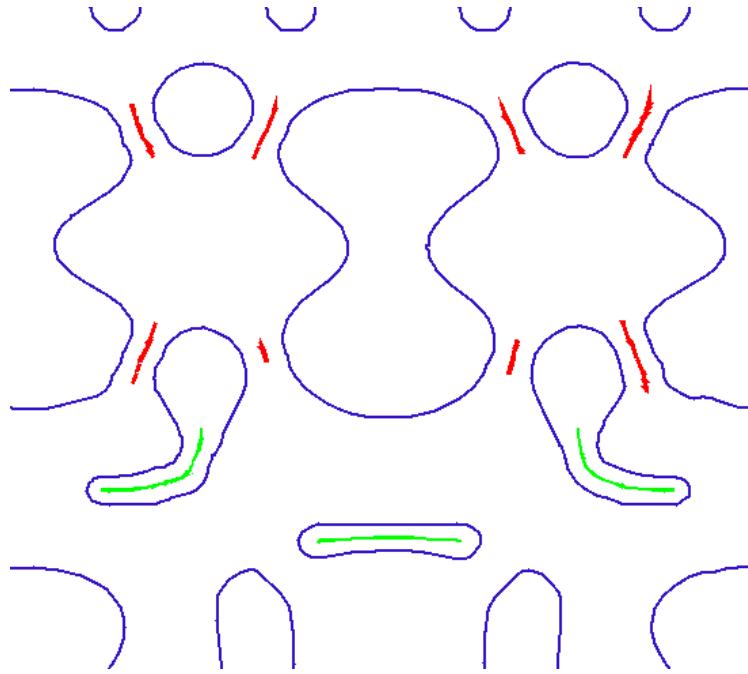


- Levelsets are a way to track a moving interface
- In our case the mask edge is the moving interface
- Curvilinear shapes are always created as an intermediate data type in the ILT flow

ILT Manufacturability

Various Levels of Mask Complexity Control Are Available

All Angle MRC



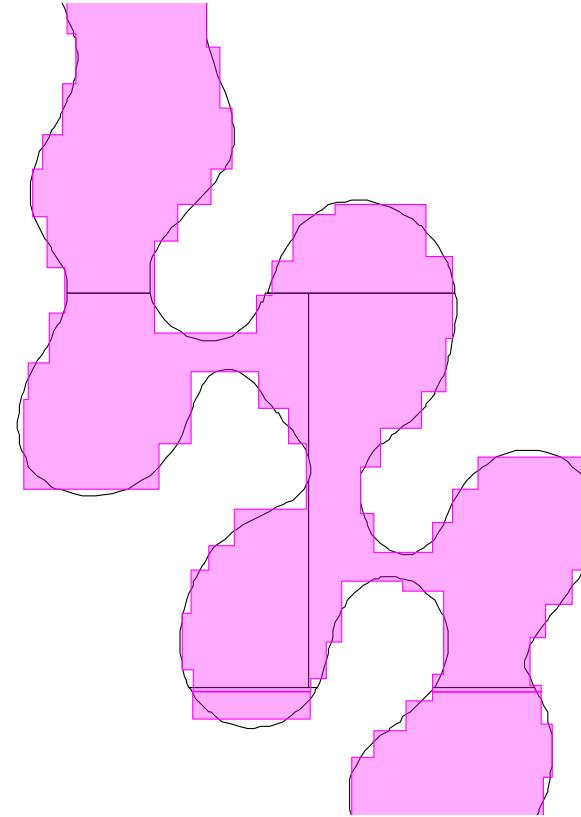
Skeletons used in MRC processing of raw mask.

Blue: raw mask edge.

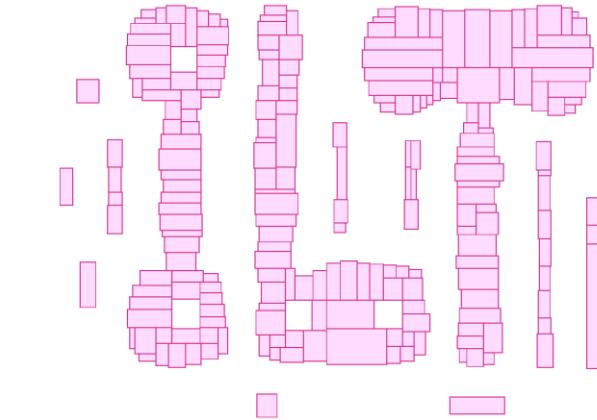
Green: interior skeleton (width).

Red: exterior skeleton (spacing).

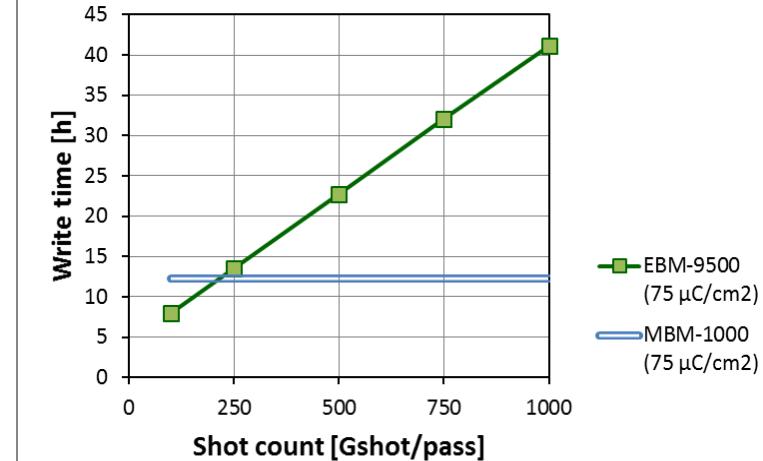
Manhattanization



Fracture/Writing



VSB vs MBM-1000 Write times



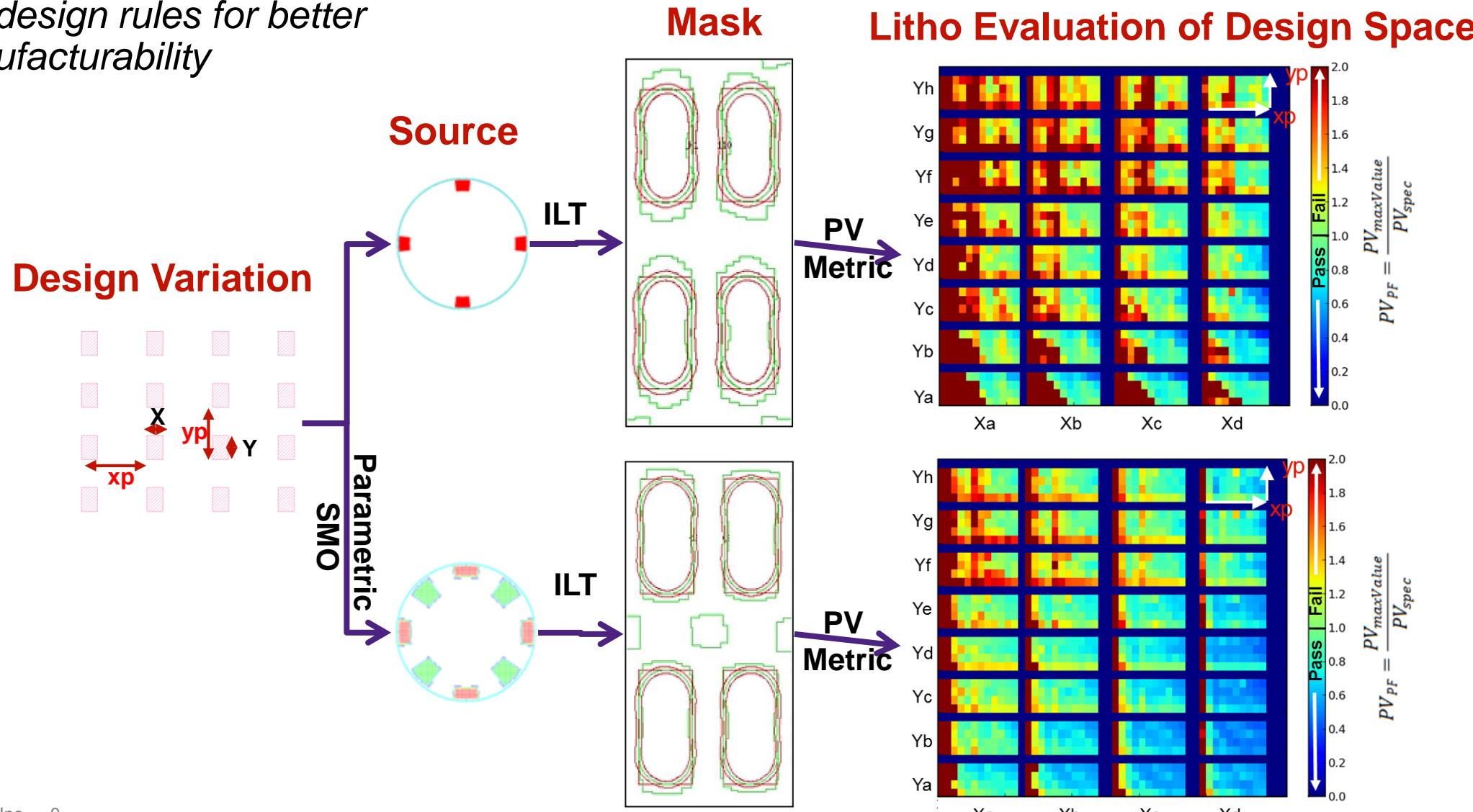
Source: NuFlare Technology
PMJ 2016

ILT Use Cases

Development, Memory, Logic

Process/Design Development: SMO & Design Exploration

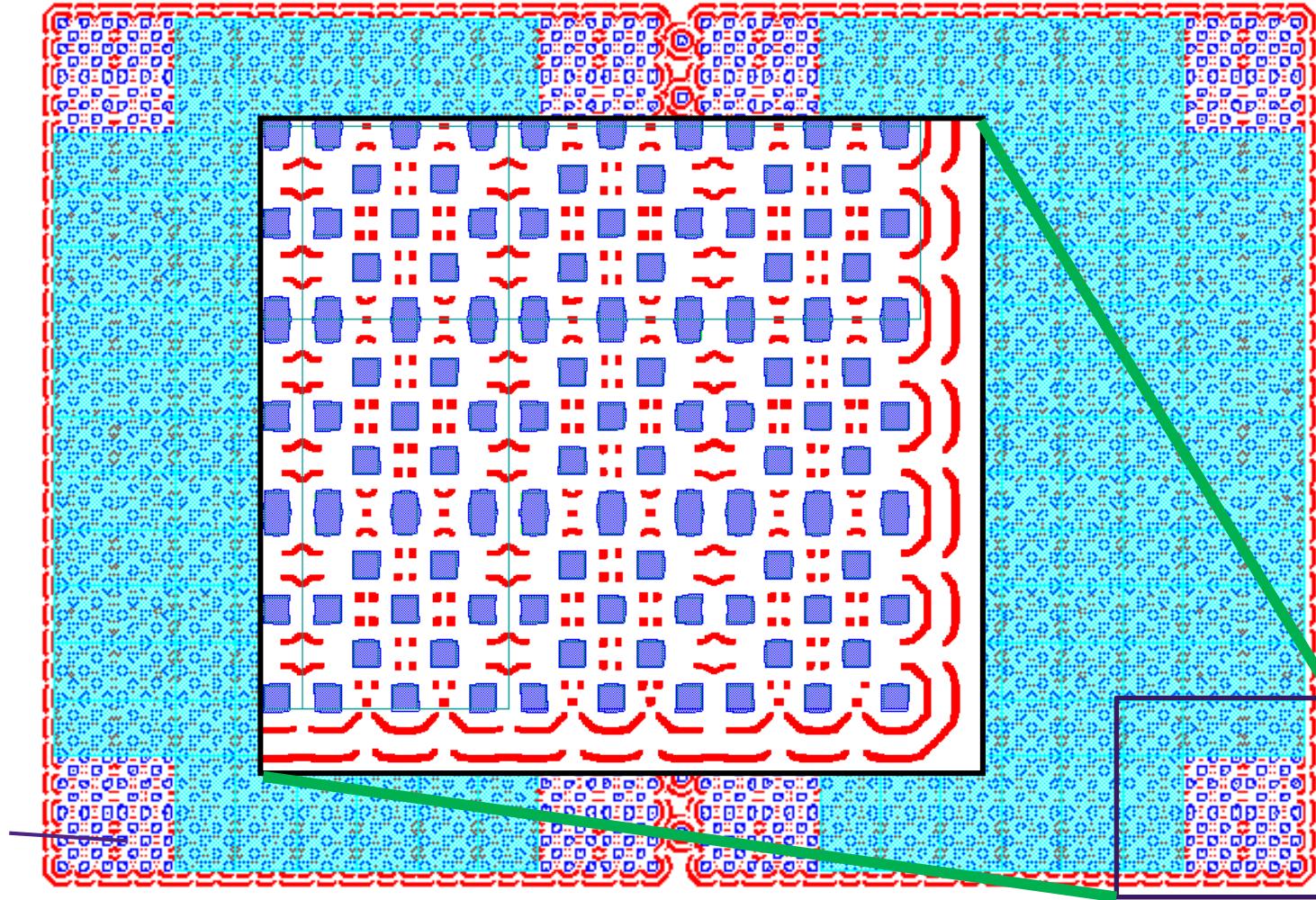
*Establishing optimal source shape
and design rules for better
manufacturability*



Memory: Cell Level ILT

Aggressive ILT for Highly Repetitive Critical Areas

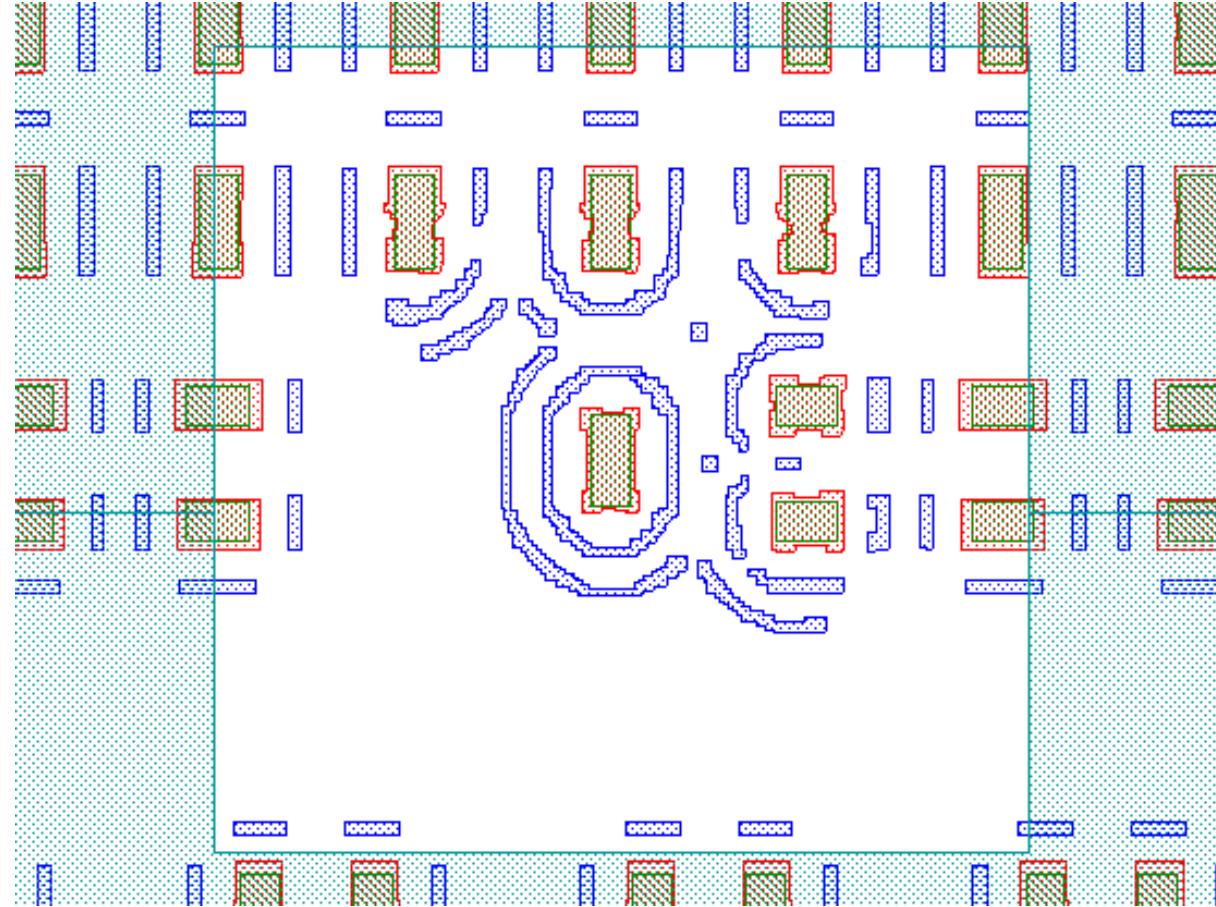
Cell Level



Memory and Logic: Hot Spot Fixing

Minimal TAT Overhead with Maximal Litho Improvement

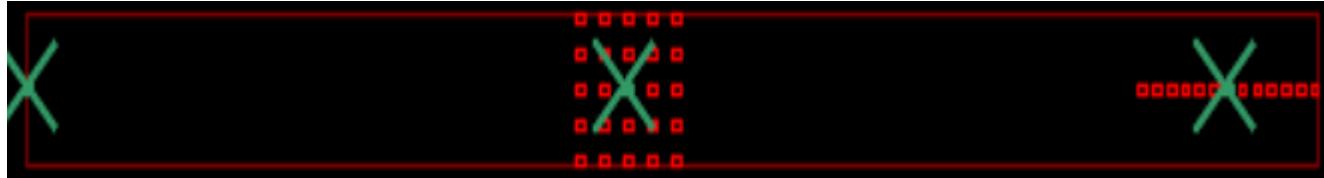
Hot Spot Fixing



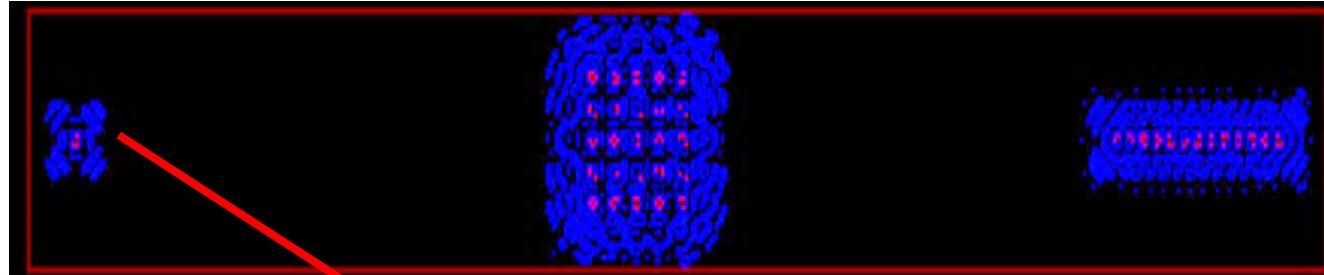
ILT Generated Rule Table For 2d Areas

ILT Guided AF Rules To Apply to Large Areas Quickly and Accurately

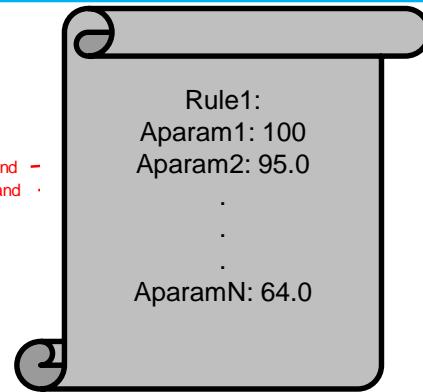
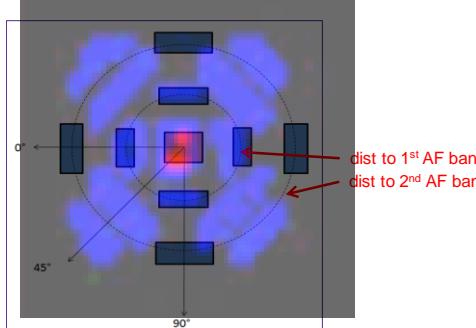
1. Mark features to be measured



2. Get ILT AFs

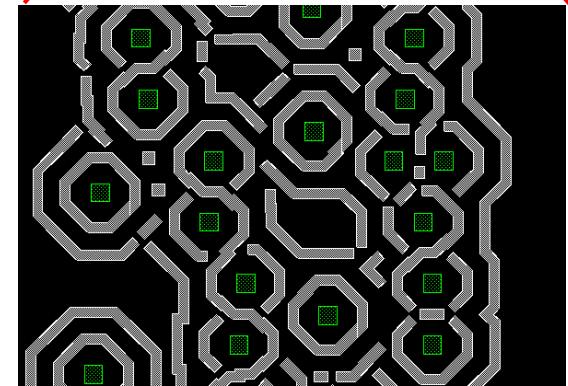
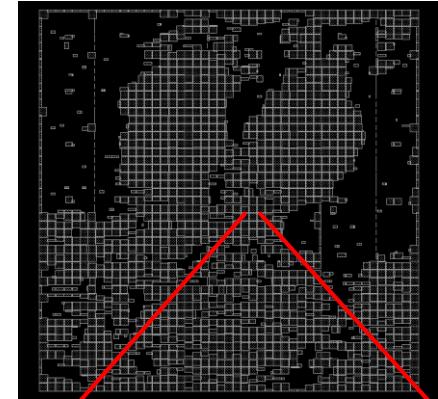


3. Create RBAF rules



RBAF2D
rule
files

4. Place Afs On Random Layout Using Rules



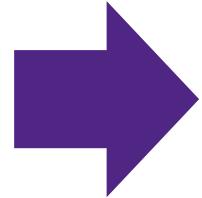
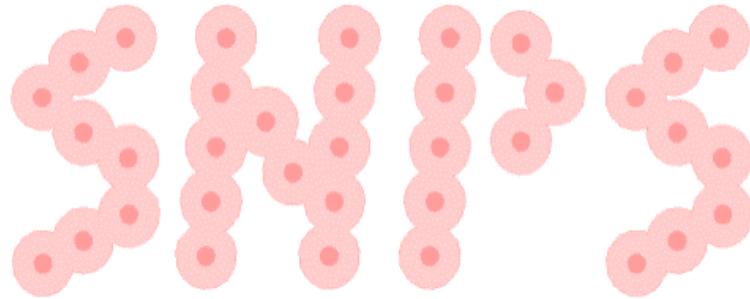
ILT Future Extensions

DSA, EUV

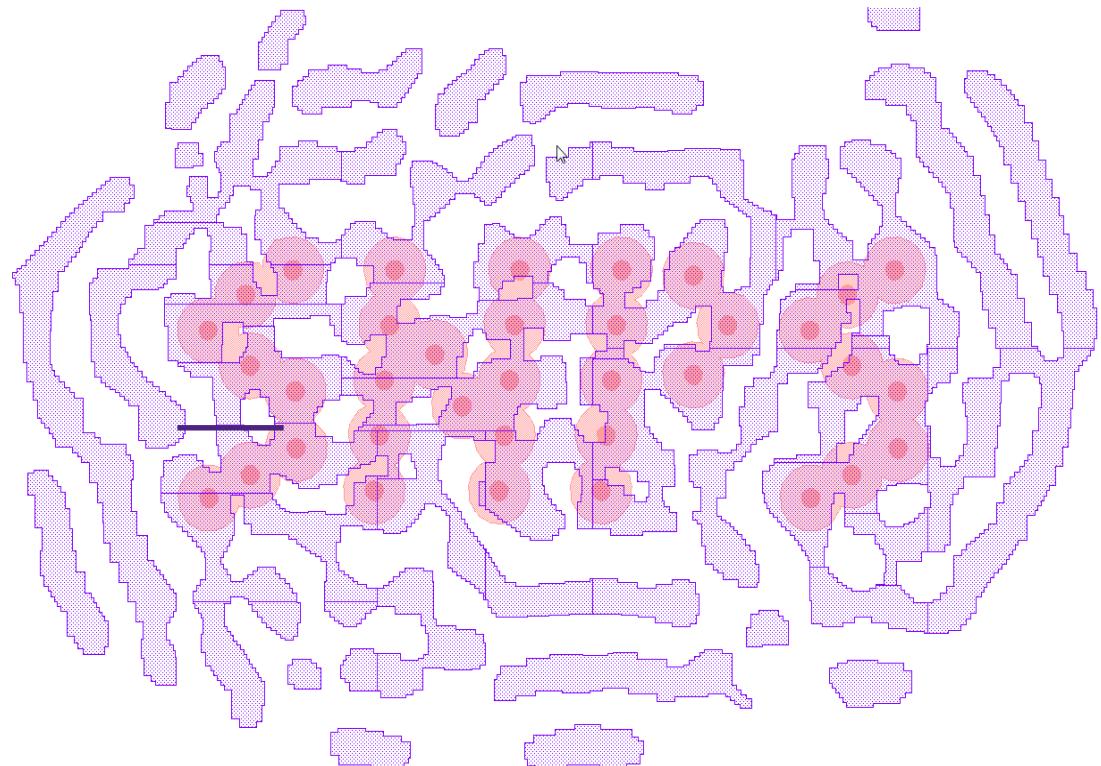
DSA Template Example

ILT Naturally Finds Merged Main and AF Solution to Resolve Overly Dense Regions

DSA-like
Freeform Target



ILT Mask



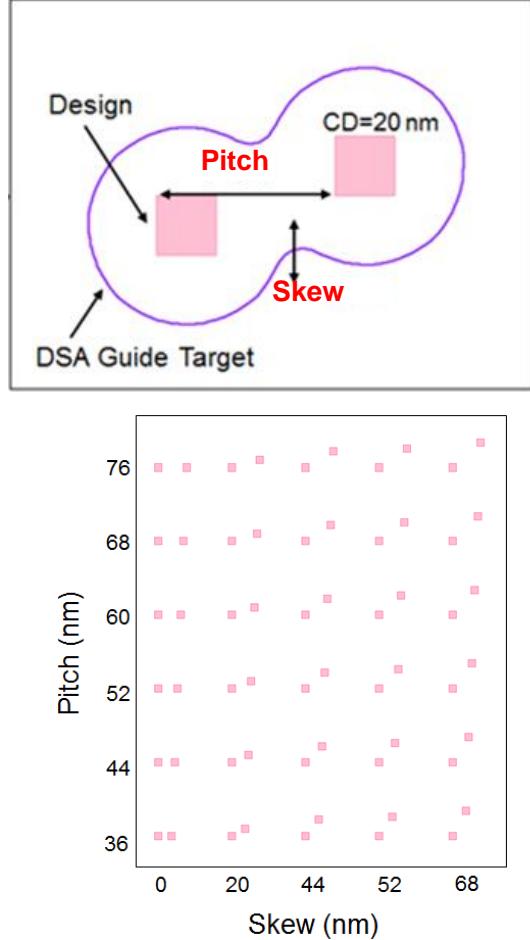
Note: difficult to distinguish MF from AF

Applying ILT for Design Exploration and Optimization,
Thuc Dam, Guangming Xiao & Kevin Lucas
LithoVision 2016

DSA Design Rule Exploration

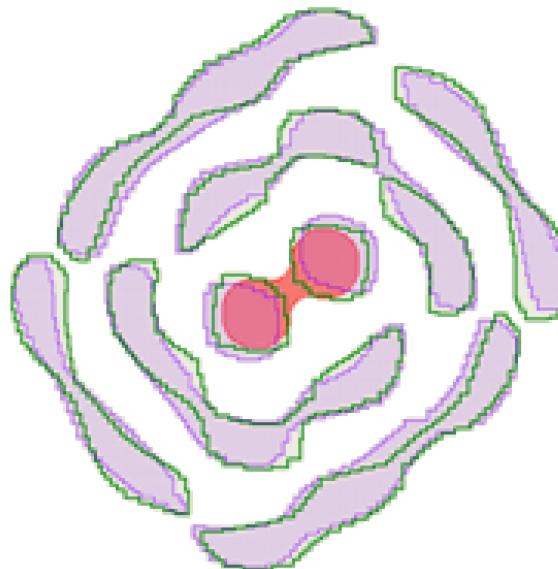
ILT Aids Development of DSA Template Design

Design Variation



Mask Variation

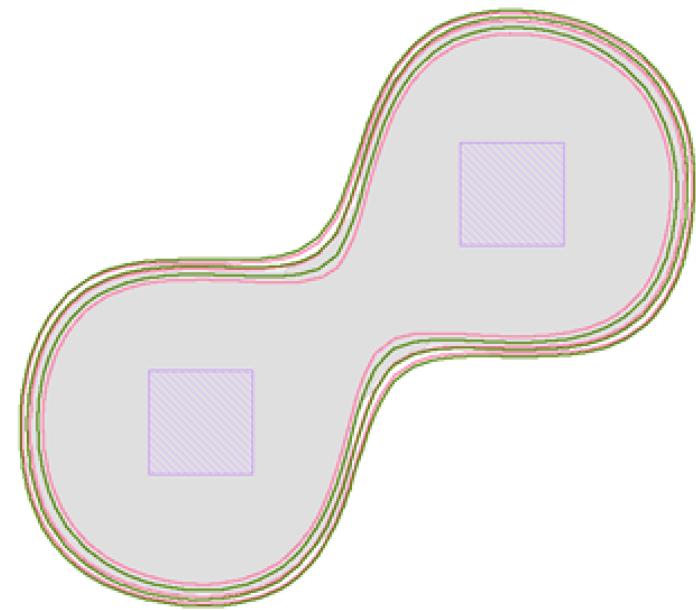
ILT



Purple – Mask w/Cost Function1
Green – Mask w/Cost Function2

Litho
Simulation

Lithographic Variation

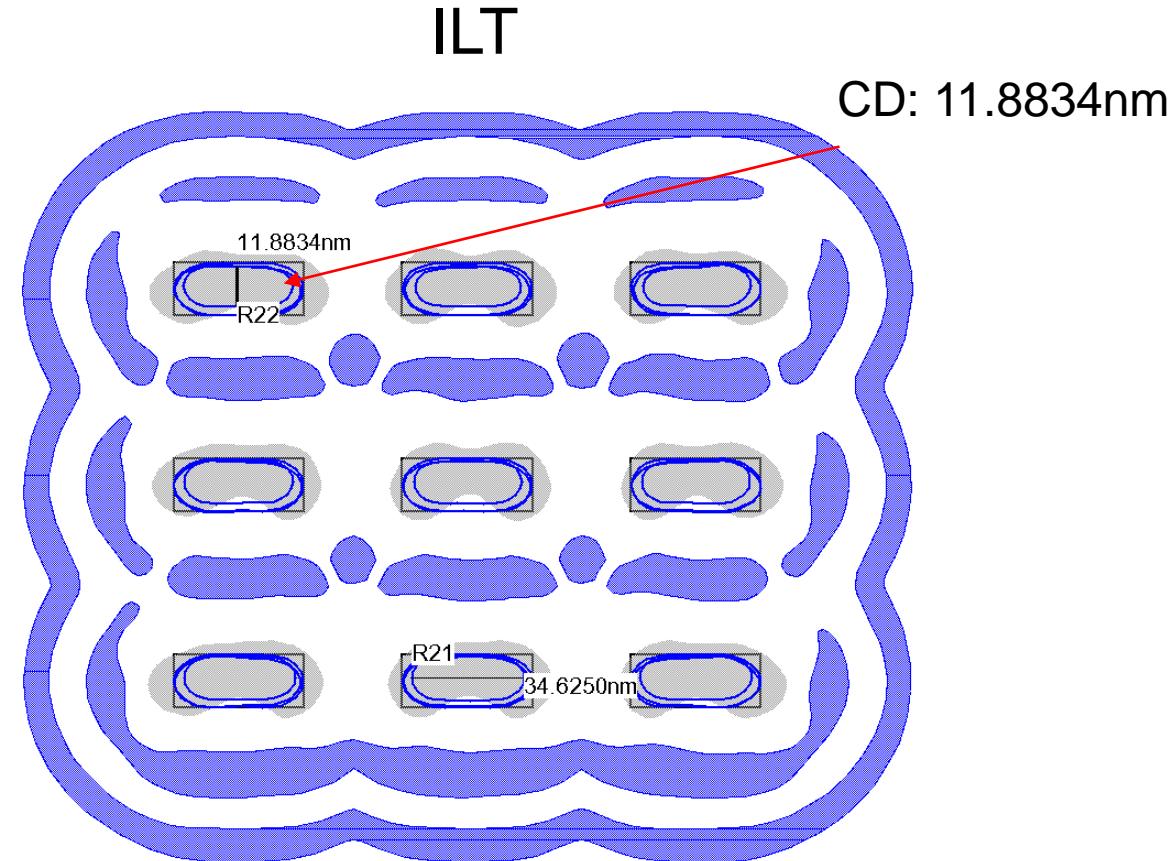
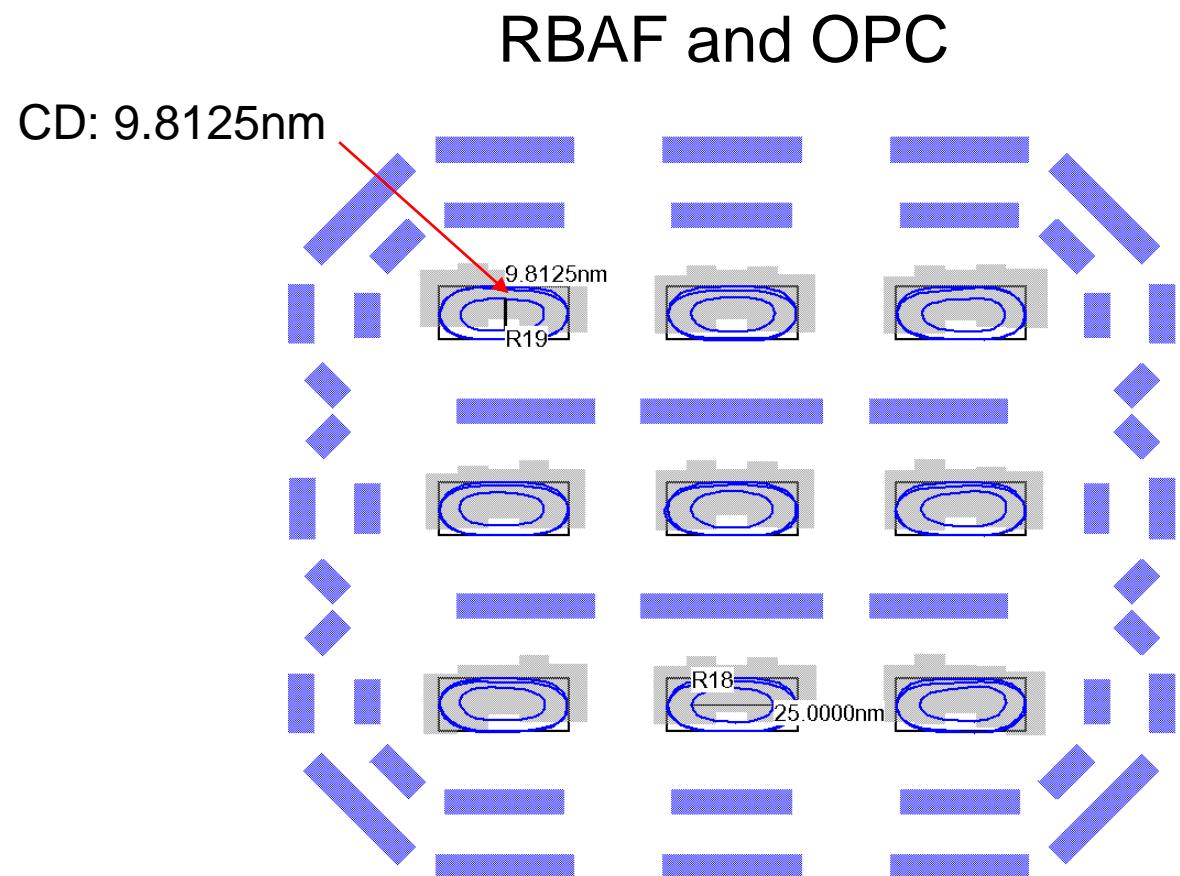


Red – PV of Mask w/Cost Function1
Green – PV of Mask w/Cost Function2

EUV 3x3 Slot Contact Array – OPC vs ILT

Asymmetric AFs Generated By ILT for PW Improvement

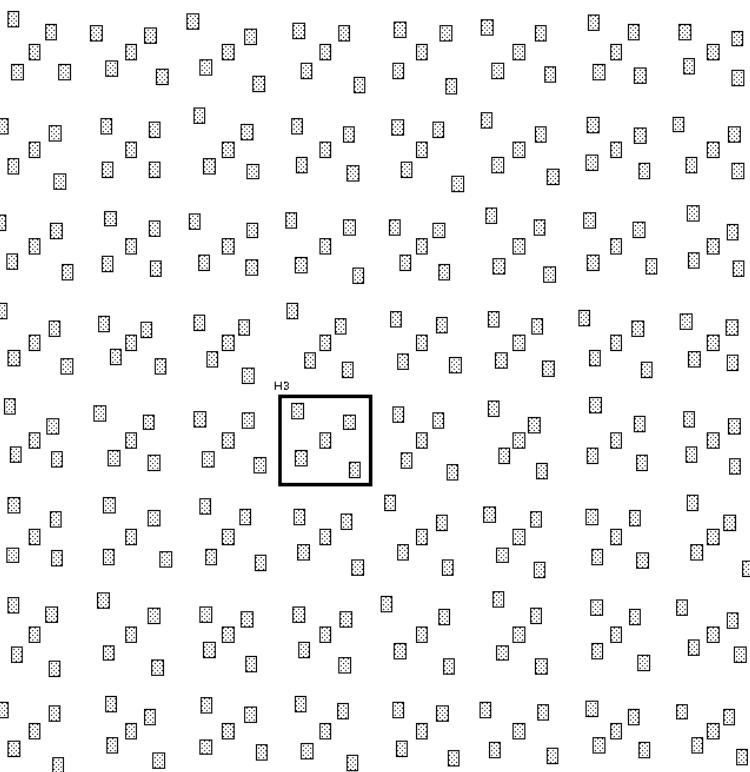
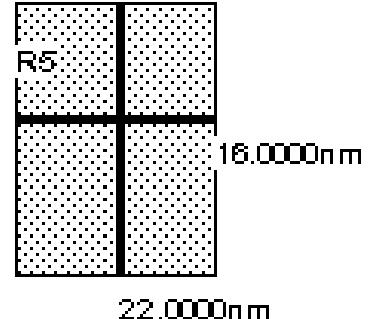
- 70nm X pitch by 60nm Y pitch
- Right edge of reticle
- Contours shown nominal, +/-50 nm defocus



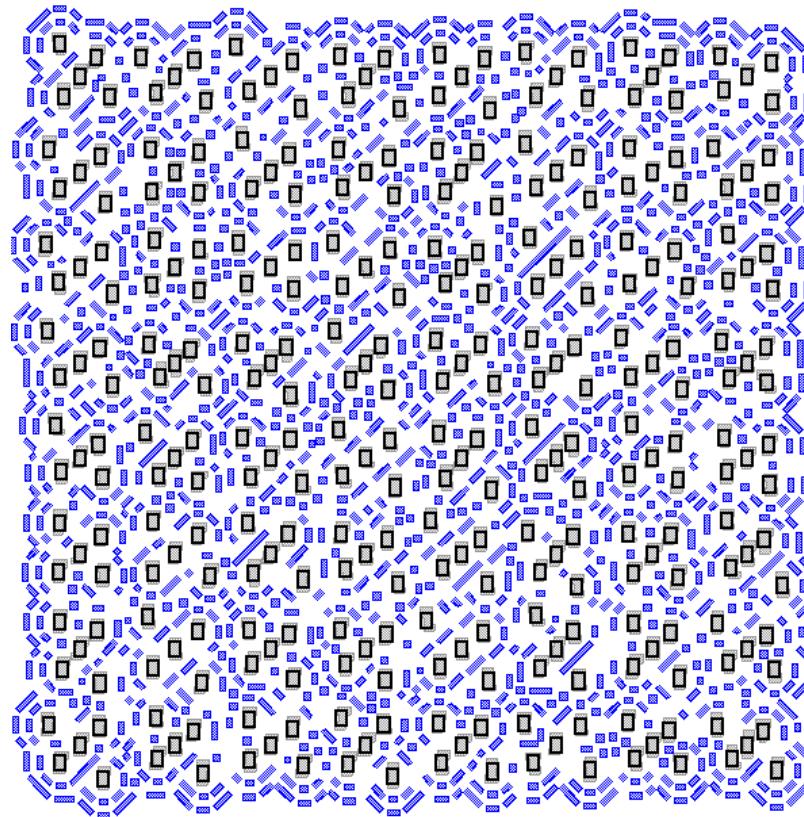
See more at: [New methodologies for lower-K1 EUV OPC and RET optimization, paper 10143-45, March 2](#)

EUV Via random pattern – PV Band improvement

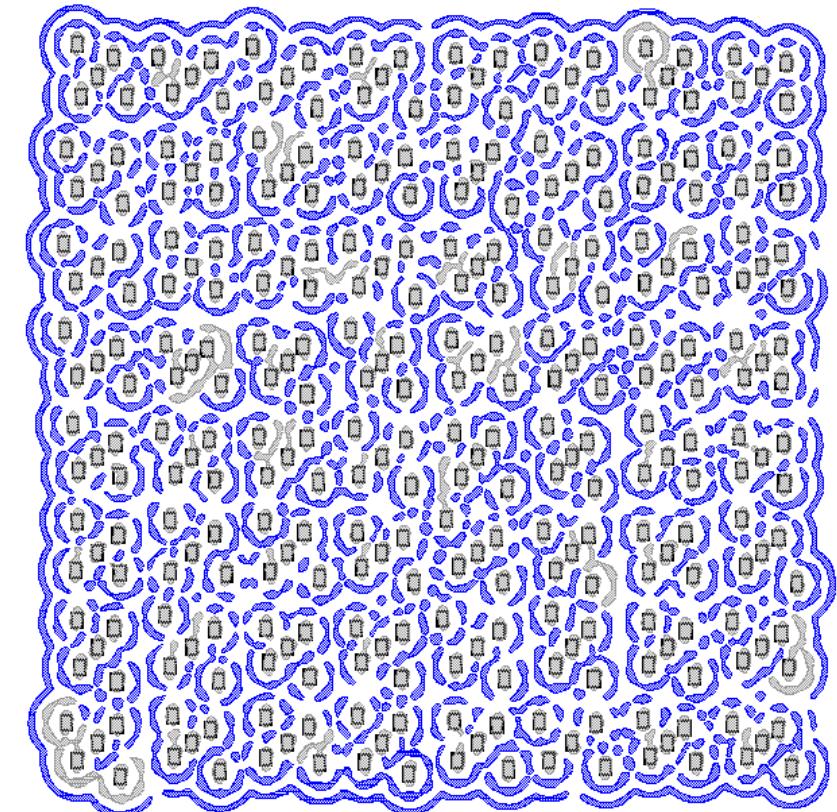
- Random via pattern – random “X” configurations of 5 contacts
- Drawn CD: 16nm x 22nm



Design



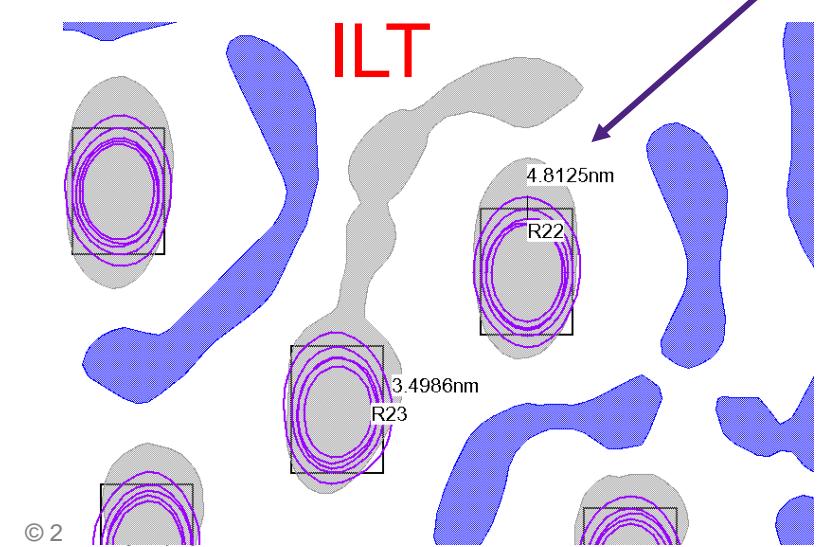
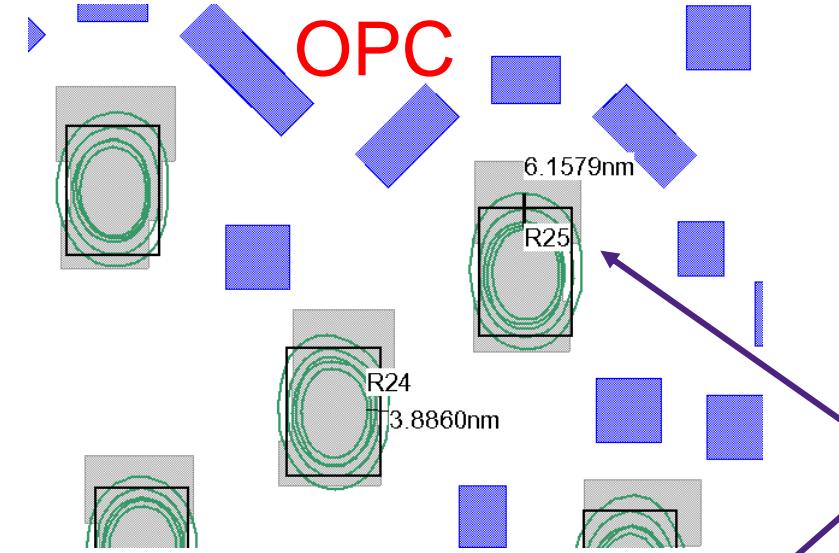
OPC



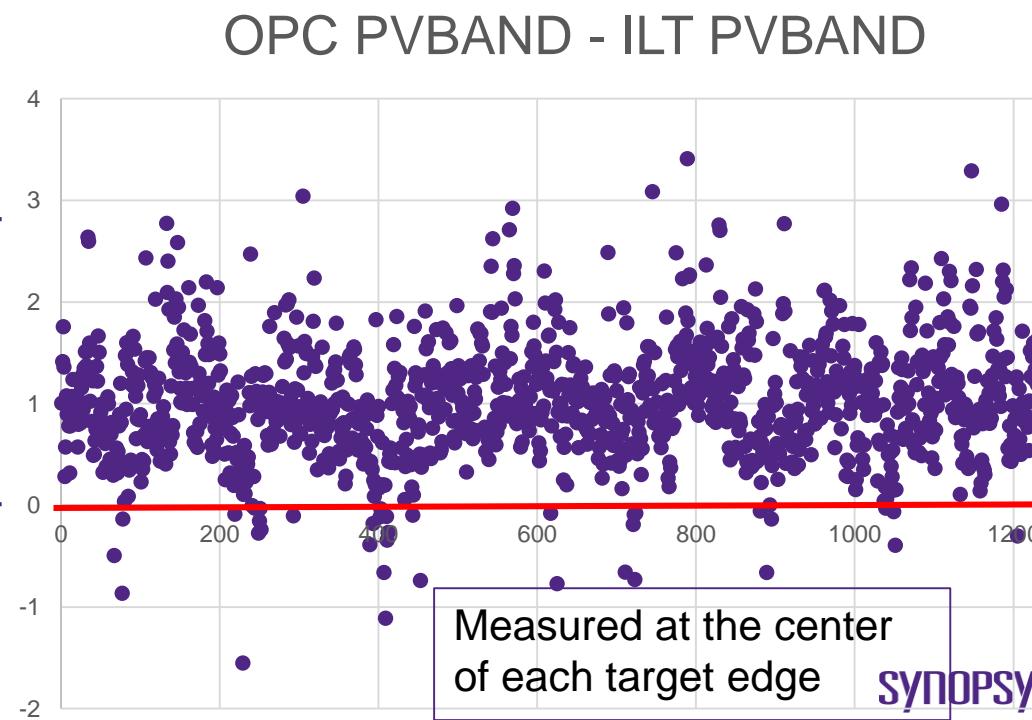
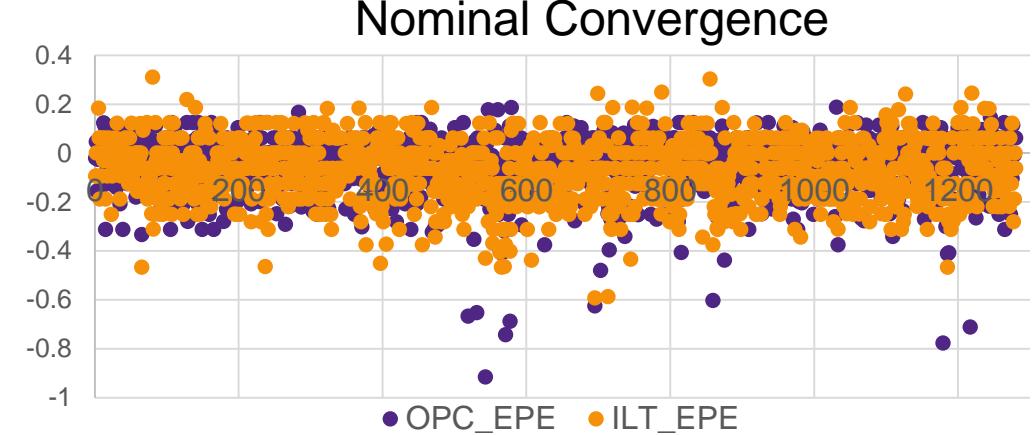
ILT

EUV Via Random Pattern – PV Band Improvement

ILT Improves PV Band by > 20%



ILT Improvement



Summary

- ILT is being used in memory and logic areas
- Shrinking MRC, design CD, and complex physical interactions make ILT more attractive
- Curvilinear ILT output is available and produces the best results
- DSA, EUV have issues that ILT can help to solve, in both development and production

Thank You

