Agency Contact:
Kelly Picasso
MCA
Tel: +1-650-968-8900, ext. 127
E-mail: kpicasso@mcapr.com

FOR IMMEDIATE DISTRIBUTION

EBEAM INITIATIVE MEMBERS COLLABORATE TO ENHANCE DESIGN FOR E-BEAM THROUGHPUT

D2S' DFEB Packed Stencil Technology and Advantest Corporation's Direct Write Lithography Equipment Increase DFEB Character Set by More Than 4X

SAN JOSE, Calif., October 1, 2009—The eBeam Initiative, a forum dedicated to the education and promotion of a new design-to-manufacturing approach known as design for e-beam (DFEB), today announced that steering group members D2S, Inc. and Advantest Corporation have collaborated to enhance throughput to make maskless system-on-chips (SoCs) feasible for prototypes and low-volume designs. Specifically, D2S has introduced its design for e-beam (DFEB) packed stencil technology, which works in conjunction with Advantest Corporation's e-beam direct write (EbDW) lithography equipment. D2S' packed stencil technology increases the number of characters available for a given layer, which in turn, reduces shot count. This allows fabs using Advantest's EbDW equipment to improve throughput for DFEB designs implemented with packed stencil technology.

D2S' proprietary DFEB solution works with character or cell projection (CP) capability on EbDW machines. The characters on a stencil mask are co-designed with a DFEB standard cell library overlay so that any design using that library will have a matching stencil mask in the EbDW machine. The stencil mask on the EbDW machine allows these complex patterns to be written on the wafer in a single shot, achieving an order-of-magnitude improvement in EbDW write times.

The packed stencil technology lays out the characters on the stencil mask to pack more in the same space than was previously possible. By co-designing the DFEB overlay library along with the stencil mask, D2S can customize the placement of the characters on a stencil mask that is optimized for each set of characters. The number of characters available in a character block for writing any given layer of a design increases substantially, making DFEB more effective and allowing the direct writing of wafers to be faster. Advantest and D2S have worked together on implementing the packed stencil for the Advantest EbDW equipment and enhanced the number of characters available from the Advantest equipment from 100 to more than 250, an improvement by a factor of 2.5. The collaboration further resulted in the Advantest EbDW equipment improving the number of character blocks per stencil mask from 12 to 20. The net increase in the number of characters available on a stencil mask goes from 1,200 to 5,000, or 4X.

-more-

As cost trends associated with advanced semiconductor fabrication continue to rise, application-specific and other custom IC manufacturers are under increasing pressure to find new manufacturing approaches. Photomask costs alone are expected to double at every new node, shrinking the application range and market for these devices, as well as threatening the profit potential of future applications.

The combination of D2S' advanced DFEB technology and Advantest's existing EbDW technology provides a viable solution to these challenges without requiring a fundamental lithography shift. By enhancing today's most advanced EbDW technology, DFEB eliminates mask costs and can speed time-to-market by shortening the design-to-lithography process flow.

Haruo Matsuno, president of Advantest, stated, "In collaboration with D2S, Advantest is now able to offer a viable e-beam direct-write solution with dramatically enhanced throughput. This technological leap forward quadruples the characters available to our F3000 lithography tool, vastly improving its throughput over what was previously possible. We look forward to furthering our relationship with D2S as we continue to enhance the effectiveness of our e-beam direct-write solutions for the low-volume high-mix SoC business, among other applications."

About The eBeam Initiative

The eBeam Initiative provides a forum for educational and promotional activities regarding a new design-to-manufacturing approach, known as design for e-beam (DFEB). DFEB reduces mask costs for semiconductor devices by combining design, design software, manufacturing, manufacturing equipment and manufacturing software expertise. The goals of the Initiative are to reduce the barriers to adoption to enable more integrated circuit (IC) design starts and faster time-to-market while increasing the investment in DFEB throughout the semiconductor ecosystem. Members and advisors, which span the semiconductor ecosystem, include: Advantest, Alchip Technologies, Altos Design Automation, Cadence Design Systems, CEA/Leti, D2S, Dai Nippon Printing, Marty Deneroff from D. E. Shaw Research, e-Shuttle, Jack Harding from eSilicon Corporation, Fastrack Design, Fujitsu Microelectronics, GenISys GmbH, Magma Design Automation, Colin Harris from PMC-Sierra, Riko Radojcic from Qualcomm, STMicroelectronics, Tela Innovations, Toppan Printing, Virage Logic and Vistec Electron Beam Lithography Group. Membership is open to all companies and institutions throughout the electronics industry. To find out more, please visit www.ebeam.org.

About D2S

D2S is empowering an era of new business opportunities for electronic products by making low-volume silicon production cost effective at the 65 nanometer node and below. D2S' advanced design-for-e-beam (DFEB) design and software capabilities maximize existing e-beam technology to virtually eliminate the costs of masks and speed time to market by shortening the design-to-lithography process flow. Headquartered in San Jose, Calif., the company was founded in 2007. For more information, see http://www.direct2silicon.com/.

About Advantest

Advantest Corporation is a world leading automatic test equipment supplier to the semiconductor industry, and also produces electronic instruments and systems. A global company, Advantest has long offered total ATE solutions, and serves the industry in every component of semiconductor test: tester, handler, mechanical and electrical interfaces, and software. Its logic, memory, mixed-signal and RF testers and device handlers are integrated into the most advanced semiconductor production lines in the world. Founded in Tokyo in 1954, Advantest established its first subsidiary in 1982, in the USA, and now has subsidiaries worldwide. Among them, Advantest America, Inc. is based in Santa Clara, Calif., Advantest Europe GmbH is based in Munich, Germany, and Advantest Taiwan Inc. is based in Hsinchu, Taiwan. More information is available at *www.advantest.co.jp*.

###